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(54) **PWM power amplifier with digital input**

PWM Leistungsverstärker mit digitalem Eingang

Amplificateur de puissance à modulation de largeur d'impulsion avec une entrée pour un signal numérique

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to high efficiency low frequency amplifiers, commonly referred to as class-D amplifiers and particularly though not exclusively to class-D audio amplifiers.

BACKGROUND OF THE INVENTION

[0002] The efforts for reducing energy consumption, weight and size of heat sinks of manufacturers of consumer apparatuses, for example in the field of car entertainment, have generated a demand for power amplifiers with a greater efficiency than the traditional class-AB amplifiers.

[0003] So-called class-D amplifiers have been proposed to respond to these requisites. Substantially, these amplifiers include a DC to AC converter circuit (DAC), which produces a PWM output signal. This PWM signal drives output power devices that through a passive lowpass filter for reconstructing an amplified analog (audio) signal drive a load (for example a speaker) that may be a part of the lowpass filter.

[0004] The analysis of the behavior of a single ended amplifier with an analog input and a PWM output (a class-D amplifier) is described in the paper "Analysis of a quality class-D amplifier", F. A. Himmelstoss, et al., I. E.E.E. Transactions on Consumer Electronics, Vol. 42, No. 3, August 1996.

[0005] On the other hand, the increasing interest in digital audio signal processing will make more convenient in many occasions to use digital amplifiers rather than analog amplifiers.

[0006] Presently, there are no known commercial applications of digital input amplifiers but few articles that describe possible design approaches:

- "Noise shaping and Pulse-Width Modulation for All-Digital Audio Power Amplifiers" by J.M. Goldberg and M.B. Sandler, Journal Audio Eng. Doc., Vol. 39, No. 6, 1991 June. This system described does not use any feedback circuit on the final stage, which to some extent penalizes the performance in terms of distortion and noise rejection. The performance appears to be strictly dependent on the characteristics of the components of the power stage (Fig. 8);
- "All digital Power Amplifier Based on Pulse Width Modulation" by M.S. Pedersen and M. Shajaan, presented during the 96th AES convention (Audio Engineering Society), 26th February, 1st March, 1994, in Amsterdam. According to this design approach there is no feedback circuit. The system appears to be burdened by resorting to a linearized PWM;
- "A Sigma-Delta Power Amplifier for Digital Input Signals" by Klugbauer-Heilmeier presented during the 102nd AES (Audio Engineering Society) convention 22nd-25th March, 1997, in Munich. The article describes a pulse density modulation (PDM) amplifier requiring a high switching frequency besides an antialiasing filter in the feedback path.

OBJECT AND SUMMARY OF THE INVENTION

[0007] The main objective of the present invention is to devise a digital input PWM power amplifier functioning at a relatively low switching frequency in order to achieve a high efficiency, being easy to make and having a low sensitivity to the spread of the actual values of the parameters of the circuit's components, and able to function at the lowest possible driving frequency of the PCM/PWM converter, without requiring integrated lowpass filters. The only filter of the system being a lowpass filter connected in cascade of the amplifier output, which is in any case always present in switching output stages.

[0008] These important objectives are effectively attained by the amplifier of the present invention.

[0009] Essentially, the PWM power amplifier of the invention comprises an oversampling and noise shaping block receiving PCM (Pulse Code Modulation) input digital data, organized in words composed of a certain number (M) of bits and outputting PCM digital data converted into words composed of a lower number (N) of bits than the number of bits of the input data (M>N) at a multiple bit rate (Fin*k) of the bit rate (Fin) of the input data.

[0010] A first bus transmits a first fraction (P) of most significant bits (MSB) of the words output from the first block and a second bus transmits the remaining (S) least significant bits (LSB) of the words output from said first block.

[0011] Each of the first and second PCM/PWM converters, fed with data transmitted on the first and on the second bus, respectively, is composed of a counter that is reset by the transitions of the digital value of data fed to the respective converter. The converter functions in an up/down mode and is fed with at least a clock signal (Fclock) whose frequency is equal to the multiplied bit rate (Fin*k) of the data transmitted on the respective bus of the converter multiplied by the base 2 raised to the relative number of bits two (P or S) of the transmitted words and generate reference digital words composed by the respective number of bits (P or S), representing incremental and decremental digital values, defining single or multiple slope rising and descending ramps of digital values, whose rate is identical to the bit rate of the data fed to the converter. A digital comparator receives through a first input the reference digital words generated by the up-down counter and through a second input the input data and outputs a PWM digital signal (MSBdlg, LSBdig) at a switching frequency equal to the bit rate of the input digital data stream.

[0012] The PWM output signal (MSBdig) of the first

converter that receives the fraction (P) of most significant bits is summed on the inverting input node (-) of a final power amplifying stage of the amplifier to the PWM output signal (LSBdig) of the second converter (LSBdig), preventively attenuated by a ratio equivalent to the base 2 raised to the number (S) of bits transmitted through the second bus to the input of the second converter.

[0013] The pair of PCM/PWM converters may be of the single or multiple ramp type.

[0014] The use of double ramp converters, that is with a succession of rising and falling ramps (that is a reference signal substantially of triangular waveform) enhances the amplifier performance in terms of distortion and of signal to noise ratio, compared to a single ramp converter (that is using a saw-tooth reference signal).

[0015] The output signal produced by the single final power stage in the case of a single ended amplifier or of the two final power stages in the case of a bridge configuration, that is, upstream of the lowpass analog signal reconstructing filter(s), is a PWM signal whose frequency is equal to the output signal (MSBdig) produced by the first converter but having a different duty-cycle in function of the following parameters:

a) supply voltage of the final power stage;
b) nonlinearity and losses of the final power stage;
c) correction made to the signal (LSBdig) output by the second converter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The various aspects and advantages of the invention will become even more evident through the following description of several embodiments and by referring to the annexed drawings, wherein:

Figure 1 is a block diagram of the basic structure of the PWM power amplifier of the invention, according to a first embodiment;
Figure 2 shows the internal structure of the final power stage;
Figure 3 shows the internal structure of each of the two PCM/PWM converters, according to a single ramp embodiment;
Figure 4 shows the operation waveforms of the PCM/PWM single ramp converter;
Figure 5 is a block diagram of the basic structure of the amplifier of the invention according to an alternative embodiment relative to the use of double ramp PCM/PWM converters;
Figure 6 shows the internal structure of the PCM/PWM double ramp converter;
Figure 7 shows the operation waveforms of the double ramp PCM/PWM converter;
Figure 8, 9, 10 and **11** show different embodiments of a bridge amplifier according to the present invention.

DESCRIPTION OF SEVERAL EMBODIMENTS OF THE INVENTION

[0017] By referring to the basic scheme of Fig. 1, each digital M bit word of the digital input data stream with a (Fin) bit rate, is converted by way of oversampling and noise shaping techniques into an N bit word of a lower number of bits than the input words (M>N) and with a multiple bit rate, Fin*k.

[0018] The N bits that compose the output words of the noise shaping and oversampling block are divided on two distinct buses. The first bus transmits a first fractional number P of most significant bits (MSB) while he second bus transmits the remaining number S of least significant bits (LSB).

[0019] The most significant bits (MSB) are sent to a first PCM/PWM converter whereas the S least significant bits (LSB) are sent to a second PCM/PWM converter.

[0020] The subdivision of the N bits into which the M bit PCM input digital data are reorganized permits to employ clock frequencies not excessively high when converting the PCM data to a PWM signal. Indeed, assuming a transformation into a PWM signal of a 16 bit PCM signal at 44.1 kHz without a detectable degradation of the signal/noise ratio, it would be necessary to use a sampling clock of $44100 \cdot 2^{16} = 2.8$GHz, which is substantially beyond the possibilities of implementation in present integrated circuits.

[0021] Another problem that is overcome by such subdivision is that the switching frequency of the output PWM signal, that for the example considered is 44.1 kHz, would be in any case too close to the maximum frequency to be played-back (generally of about 20kHz in an audio system), causing problems of harmonic distortion, of linearity and of signal residues with the PWM switching frequency downstream of the reconstructing lowpass filter.

[0022] Considering that the switching frequencies of PWM amplifiers are commonly comprised between 100Hz and 500kHz, and assuming a switching frequency of the PWM signal sufficiently far from the audio band, for example about $44100 \cdot 8 = 352.8$kHz, with a number P of MSB equal to 6 and the number S of LSB equal to 6, the clock frequency required by the PCM/PWM converters is $352800 \cdot 2^6 = 22.57$MHz, which may be easily handled with present fabrication techniques of integrated circuits.

[0023] Fig. 2 shows the internal structure that may be used to realize the final power amplifying block.

[0024] This class-D power amplifying module is described and illustrated in the European patent No. 98830685.8, filed on 13th November, 1998, in the name of the same applicant. The circuit does not require the generation of a reference triangular wave or any self-oscillating structures, making it usable also for analog inputs. Different inputs may be selected by a dedicated input configuration network (not shown as in the figure

it would be irrelevant in the present context).

[0025] Figures 3 and 4 show respectively the functional block diagram and the operation functioning waveforms of each PCM/PWM converter used in the amplifier scheme of Fig. 1, the signal indications being those of the first of the two converters fed through the P bit (MSB) bus.

[0026] According to this embodiment, both converters are of single ramp type. The ramp is generated by a cyclic and resettable up-counter, fed with a clock signal Fclock of a frequency equal to the product of the bit rate of the data transmitted on the respective bus and the base 2 raised to the number of bit in which the fed data are organized.

[0027] The signal output from each of the two PCM/PWM converters is a PWM signal, whose duty cycle depends on the MSB or LSB input data.

[0028] By referring to the complete diagram of Fig. 1, the pair of PWM signals obtained from the separate conversion of the two portions of bits, respectively MSBdig and LSBdig, are eventually added on the inverting input node (-) of the final power amplifying module, after the LSBdig PWM signal is attenuated, by a factor equivalent to a ratio equivalent to the base 2 raised to the number S of bits input through the second bus to the second converter.

[0029] In this way, the main PWM signal MSBdig, generated produced by the first PCM/PWM converter, drives by the output stage determining a switching frequency equal to Fin*K. On the other hand, the attenuated PWM signal LSBdig generated by the second converter PCM/PWM drives the output stage with a weight reduced by $1/2^S$ and thereby it does not affect the switching frequency of the output power stage but modulates the output PWM signal compensating for nonlinearities and attenuating the noise introduced by the quantization of a reduced number P of bits of the main PWM signal MSBdig.

[0030] An alternative embodiment of the amplifier of the invention is shown in Fig. 5. According to this embodiment, the use of double ramp PCM/PWM converters determines a frequency of their respective PWM output signals halved in respect to the bit rate of the input PCM data.

[0031] Figures 6 and 7 show respectively the functional block diagram of the two PCM/PWM double ramp converters and the relative operation waveforms. The indications refer to the first of the two converters, fed through the P bit bus (MSB).

[0032] Fig. 6 shows the feeding of a second clock signal Fup/down with the same multiplied frequency Fin*K of the data input to the converter that synchronizes the ramp inversions.

[0033] Of course the amplifier of the invention may also be realized in the form of a bridge amplifier by using two final power amplifying stages driven in phase opposition rather than in a single ended form.

[0034] By way of example, Fig. 8 shows the diagram of a bridge version of the amplifier, wherein the required inversion is implemented by inverting the data input to the second final stage of the power amplifier.

[0035] Fig. 9 shows an alternative embodiment of a bridge amplifier of the invention with a phase shift bridge output architecture, which is relatively more complex than that of Fig. 8, though capable of providing for enhanced performances, as described and illustrated in the above cited prior European patent application No. 98830685.8

[0036] Fig. 10 shows a further embodiment of a bridge amplifier of the invention in which rather than inverting the data fed to the input of one of the pair of final power stages functioning in phase opposition, the inversion is implemented by inverting the up-down command of the respective counters of the second pair of PCM/PWM converters, such to generate triangular reference signals in phase opposition with each other.

[0037] A fourth embodiment of the bridge amplifier of the invention is illustrated in Fig. 11. According to this embodiment, the PWM signals of double frequency compared to the frequency of the main PWM signal relative to the conversion of the least significant bits are summed to the respective main PWM signals produced by the respective PCM/PWM converters fed with the most significant bits on the respective inverting input nodes of the two final power stages.

[0038] Another characteristic of the correction operated by the separate conversion of the least significant bits is a greater freedom because the correction current may be summed, subtracted or may not influence the main drive current signal relative to the conversion of most significant bits.

[0039] An advantage of a bridge embodiment of the amplifier of the invention is that the correction signal does not contain tones at the PWM switching frequency nor at frequencies near the switching frequency. Notably, tones in a ± 20 kHz band centered on the switching frequency are brought back in base band, causing an increase of the distortion and/or of noise.

[0040] In all the embodiments shown in the figures, is indicated the use of simple resistors for coupling PWM signals to the inverting input of the final power stage or stages (RMSB, RLSB, ...); however, as it will be evident to the skilled person these coupling resistors may be substituted by current generators driven by the logic signal output by the respective PCM/PWM converters.

Claims

1. A digital input PWM power amplifier comprising:

   an oversampling and noise shaping circuit receiving pulse code modulated (PCM) digital input data organized in words of a first number M of bits at a certain bit rate Fin and outputting pulse code modulated digital data organized in

words of a smaller number N of bits at a multiple bit rate Fin*K;
a first bus transmitting a first number (P) of most significant bits (MSB) of said N bit words output from said first circuit and a second bus transmitting a second number (S) of least significant bits of said N bit words output from said first circuit;
first and second PCM/PWM converters, respectively fed with said first and second number of bits transmitted through said first and said second bus, each converter including a counter driven by a clock signal (Fclock) of frequency equal to the product of the bit rate Fin*K of the MSB and LSB bits transmitted on the respective bus and the base 2 raised to the respective number of bits (P, S) generating reference digital words composed of said respective number of bits (P, S), defining ramps of digital values with a frequency identical to said multiple bit rate Fin*K, and a digital comparator receiving through a first input said reference digital words and through a second input the respective first and second number of bits (MSB, LSB) and outputting a respective PWM signal (MSBdig, LSBdig);
the PWM signal MSBdig output by said first converter, being summed to an attenuated version of the PWM signal (LSBdig) output by said second converter on the inverting input node (-) of an output power stage.

2. The PWM amplifier according to claim 1, **characterized in that** said first and second PCM/PWM converters are of the single ramp type.

3. The PWM amplifier according to claim 1, **characterized in that** said first and second PCM/PWM converters, are of the double ramp type, said counter being of the up/down type and generating reference digital words composed of said second number (S) of least significant bits in the form of a succession of rising and falling ramps of a halved frequency compared to said multiple bit rate Fin*k.

4. The PWM amplifier according to any of the preceding claims **characterized in that** is single ended and employs a single output power stage.

5. A PWM amplifier according to any of claims 1, 2 and 3, having an additional output power stage functioning in phase opposition to the first one in a bridge arrangement in which the inversion of the driving signal to the inverting input of one of the two power stages is realized by inverting the PWM signals output by said pair of PCM/PWM converters.

6. A PWM amplifier according to any of the claims 1, 2 and 3, employing an additional output power stage functioning in phase opposition to the first one in a bridge arrangement and in which the inversion of the driving signal of one of the two power stages is realized by inverting each of said first and second buses and duplicating said pair of PCM/PWM converters.

7. A PWM amplifier according to any of the claims 1, 2 and 3 employing an additional output power stage functioning in phase opposition to the first one in a bridge arrangement in which the inversion of the driving signal fed to the inverting input of one of the two power stages is realized by duplicating said pair of PCM/PWM converters, coupling the inputs of the two converters forming said duplicated second pair of PCM/PWM converters to said first and second bus without preventively inverting them but inverting instead the ramp inversion commands (Fup-down) of the two PCM/PWM converters of said duplicated pair.

8. The amplifier according to claim 7, **characterized in that** it also comprises means for inverting the PWM signals output by the PCM/PWM converters of said two pairs of converters that are fed with said least significant bits (LSBdig), second attenuating means (RLSB2+RLSB1-) of said inverted signals and means to respectively sum said inverted and attenuated signals on the inverting input node to the signals produced by the other PCM/PWM converter of the respective pair of converters.

Patentansprüche

1. Pulsbreitenmodulationsleistungsverstärker mit digitalem Eingang, der aufweist:

eine Überabtastungs- und Rauschformungsschaltung, die pulscodemodulierte (Pulscodemodulation) digitale Eingangsdaten empfängt, die in Worte einer ersten Anzahl M von Bits mit einer bestimmten Bitrate Fin organisiert sind, und pulscodemodulierte digitale Daten ausgibt, die in Worten einer kleineren Anzahl N von Bits mit einer mehrfachen Bitrate Fin*K organisiert sind;
einen ersten Bus, der eine erste Anzahl (P) höchstwertiger Bits (MSB) der N-Bit-Worte überträgt, die aus der ersten Schaltung ausgegeben werden, und einen zweiten Bus, der eine zweite Anzahl (S) niedrigstwertiger Bits der N-Bit-Worte überträgt, die aus der ersten Schaltung ausgegeben werden;
ersten und zweite Pulscodemodulations-/Pulsbreitenmodulationswandler, die jeweils mit der ersten und zweiten Anzahl der Bits versorgt

werden, die durch den ersten und zweiten Bus übertragen werden, wobei jeder Wandler einen Zähler, der durch ein Taktsignal (Fclock) einer Frequenz betrieben wird, die gleich dem Produkt der Bitrate Fin*K der MSB- und LSB-Bits, die auf dem jeweiligen Bus übertragen werden, und der Basis 2 hoch die jeweilige Anzahl von Bits (P, S) ist, der Bezugsdigitalworte erzeugt, die aus der jeweiligen Anzahl von Bits (P, S) bestehen, die Rampen digitaler Werte mit einer Frequenz definieren, die identisch zu der mehrfachen Bitrate Fin*K ist, und einen digitalen Komparator aufweist, der durch einen ersten Eingang die Bezugsdigitalworte und durch einen zweiten Eingang die jeweilige erste und zweite Anzahl von Bits (MSB, LSB) empfängt und ein jeweiliges Pulsbreitenmodulationssignal (MSBdig, LSBdig) ausgibt;

wobei das Pulsbreitenmodulationssignal (MSBdig), das aus dem ersten Wandler ausgegeben wird, zu einer gedämpften Version des Pulsbreitenmodulationssignals (LSBdig) summiert wird, das durch den zweiten Wandler am invertierenden Eingangsknoten (-) einer Ausgangsleistungsstufe ausgegeben wird.

2. Pulsbreitenmodulationsverstärker nach Anspruch 1, **dadurch gekennzeichnet, daß** die ersten und zweiten Pulscodemodulations-/Pulsbreitenmodulationswandler aus dem Einzelrampentyp bestehen.

3. Pulsbreitenmodulationsverstärker nach Anspruch 1, **dadurch gekennzeichnet, daß** die ersten und zweiten Pulscodemodulations-/Pulsbreitenmodulationswandler aus dem Doppelrampentyp bestehen, wobei der Zähler aus dem Aufwärts-/Abwärtstyp besteht und Bezugsdigitalworte, die aus der zweiten Anzahl (S) niedrigstwertiger Bits bestehen, in der Form einer Folge von ansteigenden und abfallenden Rampen einer im Vergleich mit der mehrfachen Bitrate Fin*k halbierten Frequenz erzeugt.

4. Pulsbreitenmodulationsverstärker nach einem der vorhergehenden Ansprüche, **dadurch gekennzeichnet, daß** er unsymmetrisch ist und eine einzelne Ausgangsleistungsstufe einsetzt.

5. Pulsbreitenmodulationsverstärker nach einem der Ansprüche 1, 2 und 3, der eine zusätzliche Leistungsstufe aufweist, die in Gegenphase zur ersten in einer Brückenanordnung arbeitet, in der die Inversion des Treibersignals zum invertierenden Eingang einer der beiden Leistungsstufen durch Invertieren der Pulsbreitenmodulationssignale realisiert wird, die durch das Pulscodemodulations-/Pulsbreitenmodulationswandlerpaar ausgegeben werden.

6. Pulsbreitenmodulationsverstärker nach einem der Ansprüche 1, 2 und 3, der eine zusätzliche Ausgangsleistungsstufe einsetzt, die in Gegenphase zur ersten in einer Brückenanordnung arbeitet und in der die Inversion des Treibersignals einer der beiden Leistungsstufen durch Invertieren jedes der ersten und zweiten Busse und Verdoppelung des Pulscodemodulations-/Pulsbreitenmodulationswandlerpaares realisiert wird.

7. Pulsbreitenmodulationsverstärker nach einem der Ansprüche 1, 2 und 3, der eine zusätzliche Ausgangsleistungsstufe einsetzt, die in Gegenphase zur ersten in einer Brückenanordnung arbeitet, in der die Inversion des Treibersignals, das dem invertierenden Eingang einer der beiden Leistungsstufen zugeführt wird, durch Verdopplung des Pulscodemodulations-/Pulsbreitenmodulationswandlerpaares realisiert wird, wobei die Eingänge der beiden Wandler, die das verdoppelte zweite Pulscodemodulations-/Pulsbreitenmodulationswandlerpaar bilden mit dem ersten und zweiten Bus gekoppelt werden, ohne sie vorbeugend zu invertieren, sondern stattdessen die Rämpen-Inversionsbefehle (Fup-down) der beiden Pulscodemodulations-/Pulsbreitenmodulationswandler des verdoppelten Paars invertiert werden.

8. Verstärker nach Anspruch 7, **dadurch gekennzeichnet, daß** er außerdem eine Einrichtung zum Invertieren der Pulsbreitenmodulationssignale, die durch die Pulscodemodulations-/Pulsbreitenmodulationswandler der beiden Wandlerpaare ausgegeben werden, die mit den niedrigstwertigen Bits (LSBdig) beliefert werden, eine zweite Dämpfungseinrichtung (RLSB2+RLSB1-) der invertierten Signale und eine Einrichtung zum jeweiligen Summieren der invertierten und gedämpften Signale am invertierenden Eingangsknoten zu den Signalen aufweist, die durch den anderen Pulscodemodulations-/Pulsbreitenmodulationswandler des jeweiligen Wandlerpaars erzeugt werden.

Revendications

1. Amplificateur de puissance numérique PWM d'entrée comprenant :

un circuit de sur-échantillonnage et de mise en forme de bruit recevant des données d'entrée numériques modulées par impulsions codées (PCM) organisées en mots d'un premier nombre M de bits à un certain débit Fin et fournissant des données numériques modulées par impulsions codées organisées en mots d'un

plus petit nombre N de bits à un débit de bits multiple Fin*K ;
un premier bus transmettant un premier nombre (P) de bits les plus significatifs (MSB) des mots à N bits fournis à partir du premier circuit et un second bus transmettant un second nombre (S) de bits les moins significatifs (LSB) desdits mots à N bits fournis par le premier circuit ;
des premier et second convertisseurs PCM/PWM, recevant respectivement les premier et second nombres de bits transmis par les premier et second bus, chaque convertisseur contenant un compteur piloté par un signal d'horloge (Fclock) de fréquence égale au produit du débit de bits Fin*K des MSB et LSB transmis sur le bus respectif et la surélévation en base 2 au nombre respectif de bits (P, S) produisant des mots numériques de référence constitués du nombre respectif de bits (P, S) définissant des rampes de valeurs numériques de fréquence identique au débit de bits multiple Fin*K, et un comparateur numérique recevant par une première entrée les mots numériques de référence et par une seconde entrée les premier et second nombres respectifs de bits (MSB, LSB) et fournissant un signal PWM respectif (MSBdig, LSBdig) ;
le signal PWM (MSBdig) fourni par le premier convertisseur étant sommé en une version atténuée du signal PWM (LSBdig) fourni par le second convertisseur sur le noeud d'entrée inverseur (-) d'un étage de puissance de sortie.

2. Amplificateur PWM selon la revendication 1, **caractérisé en ce que** des premier et second convertisseurs PCM/PWM sont du type à rampe unique.

3. Amplificateur PWM selon la revendication 1, **caractérisé en ce que** les premier et second convertisseurs PCM/PWM sont du type à double rampe, le compteur étant du type compteur/décompteur et produisant des mots numériques de référence constitués du second nombre (S) de bits le moins significatif sous forme d'une succession de rampes montantes et descendantes de fréquence moitié par rapport au débit de bits multiple Fin*k.

4. Amplificateur PWM selon l'une quelconque des revendications précédentes, **caractérisé en ce qu'**il est à une seule borne et utilise un seul étage de puissance de sortie.

5. Amplificateur PWM selon l'une quelconque des revendications 1, 2 et 3, ayant un étage de puissance de sortie supplémentaire fonctionnant en opposition de phase par rapport au premier selon un montage en pont dans lequel l'inversion du signal pilote vers l'entrée inverseuse de l'un des deux étages de puissance est réalisée en inversant les signaux PWM de sortie fournis par la paire de convertisseurs PCM/PWM.

6. Amplificateur PWM selon l'une quelconque des revendications 1, 2 et 3, utilisant un étage de sortie supplémentaire fonctionnant en opposition de phase par rapport au premier selon un montage en pont et dans lequel l'inversion du signal pilote de l'un des deux étages de puissance est réalisée en inversant chacun des premier et second bus et en dupliquant la paire de convertisseurs PCM/PWM.

7. Amplificateur PWM selon l'une quelconque des revendications 1, 2 et 3, utilisant un étage de puissance de sortie supplémentaire fonctionnant en opposition de phase par rapport au premier selon un montage en pont dans lequel l'inversion du signal pilote fourni à l'entrée inverseuse de l'un des deux étages de puissance est réalisée en dupliquant la paire de convertisseurs PCM/PWM, en couplant les entrées des deux convertisseurs formant la seconde paire dupliquée de convertisseurs PCM/PWM aux premier et second bus, sans les inverser de façon préventive mais en inversant au lieu de cela les commandes d'inversion de rampe (Fup-dowm) des deux convertisseurs PCM/PWM de la paire dupliquée.

8. Amplificateur selon la revendication 7, **caractérisé en ce qu'**il comprend également un moyen pour inverser les signaux PWM fournis par les convertisseurs PCM/PWM des deux paires de convertisseurs qui reçoivent les bits les moins significatifs (LSBdig), un second moyen d'atténuation (RLSB2+RLSB1) des signaux inversés, et un moyen pour sommer respectivement les signaux inversés et atténués sur le noeud d'entrée inverseur en les signaux produits par l'autre convertisseur PCM/PWM de la paire respective de convertisseurs.

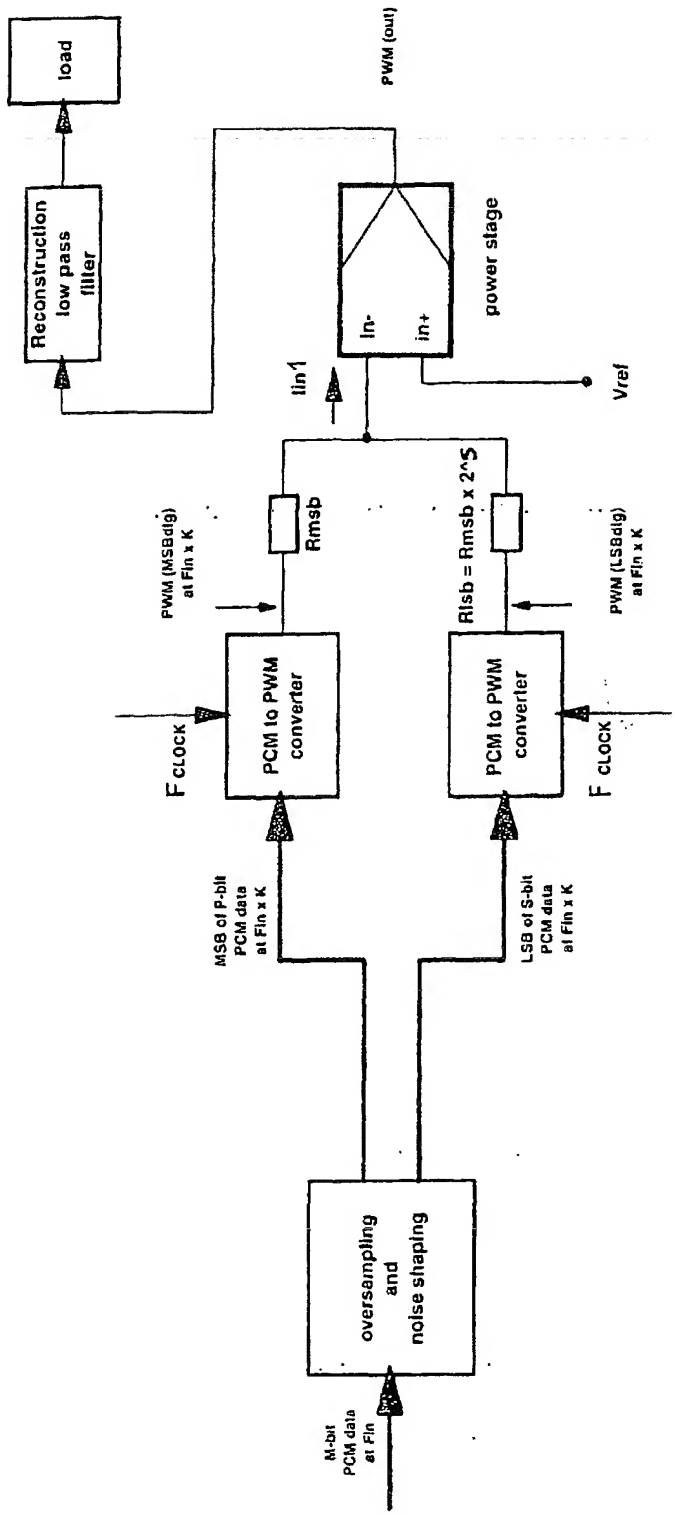
load
Reconstruction low pass filter
PWM (out)
power stage
In-
in+
Iin1
Vref
Rmsb
Rlsb = Rmsb x 2^S
PWM (MSBdig) at Fin x K
PWM (LSBdig) at Fin x K
PCM to PWM converter
PCM to PWM converter
F CLOCK
F CLOCK
MSB of P-bit PCM data at Fin x K
LSB of S-bit PCM data at Fin x K
oversampling and noise shaping
M-bit PCM data at Fin

FIG. 1

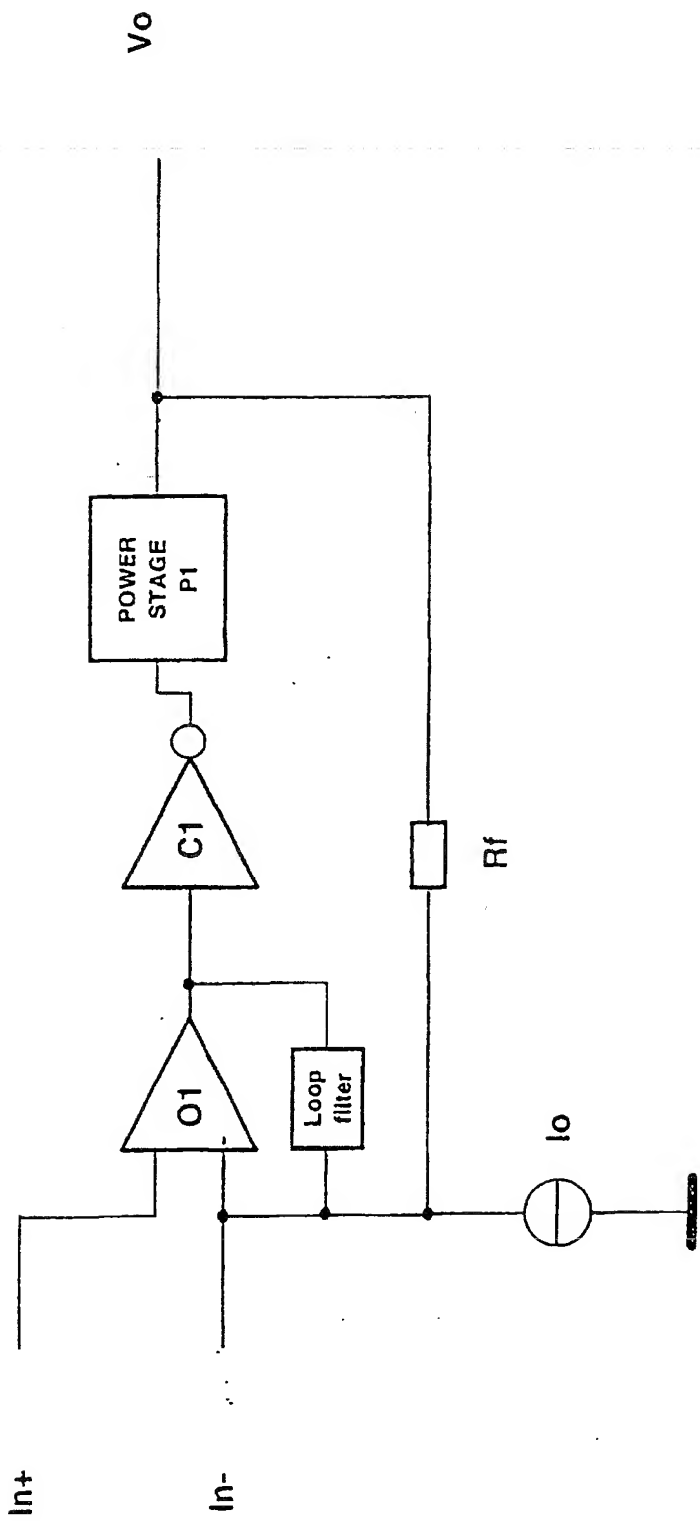

FIG. 2

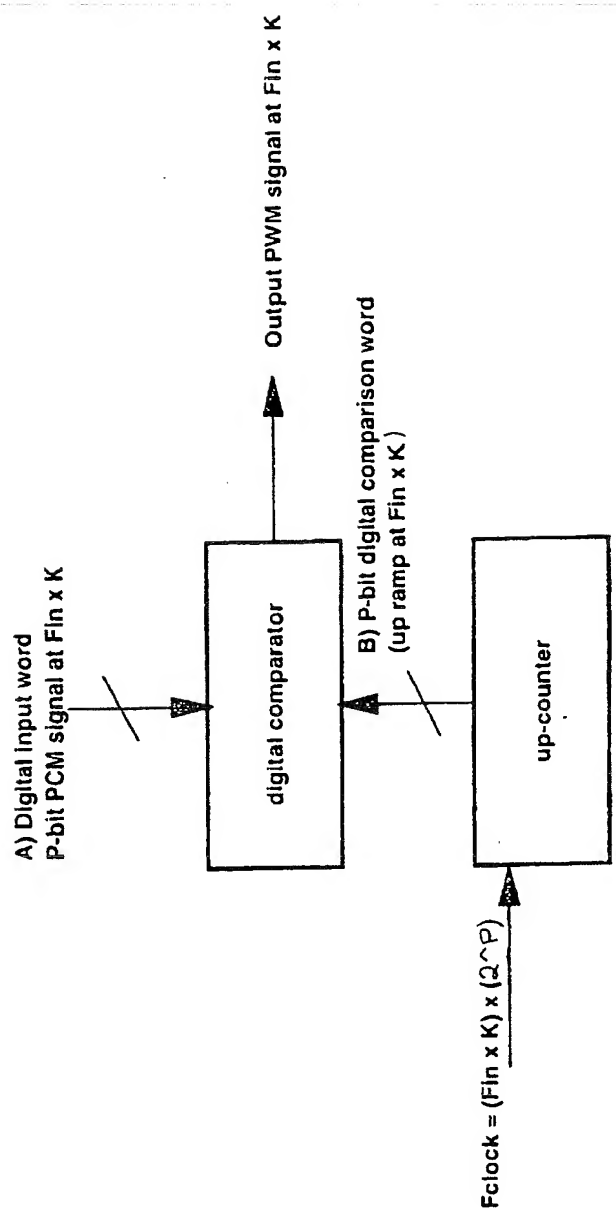
A) Digital input word
P-bit PCM signal at Fin x K
digital comparator
Output PWM signal at Fin x K
B) P-bit digital comparison word
(up ramp at Fin x K)
up-counter
Fclock = (Fin x K) x (2^P)

FIG. 3

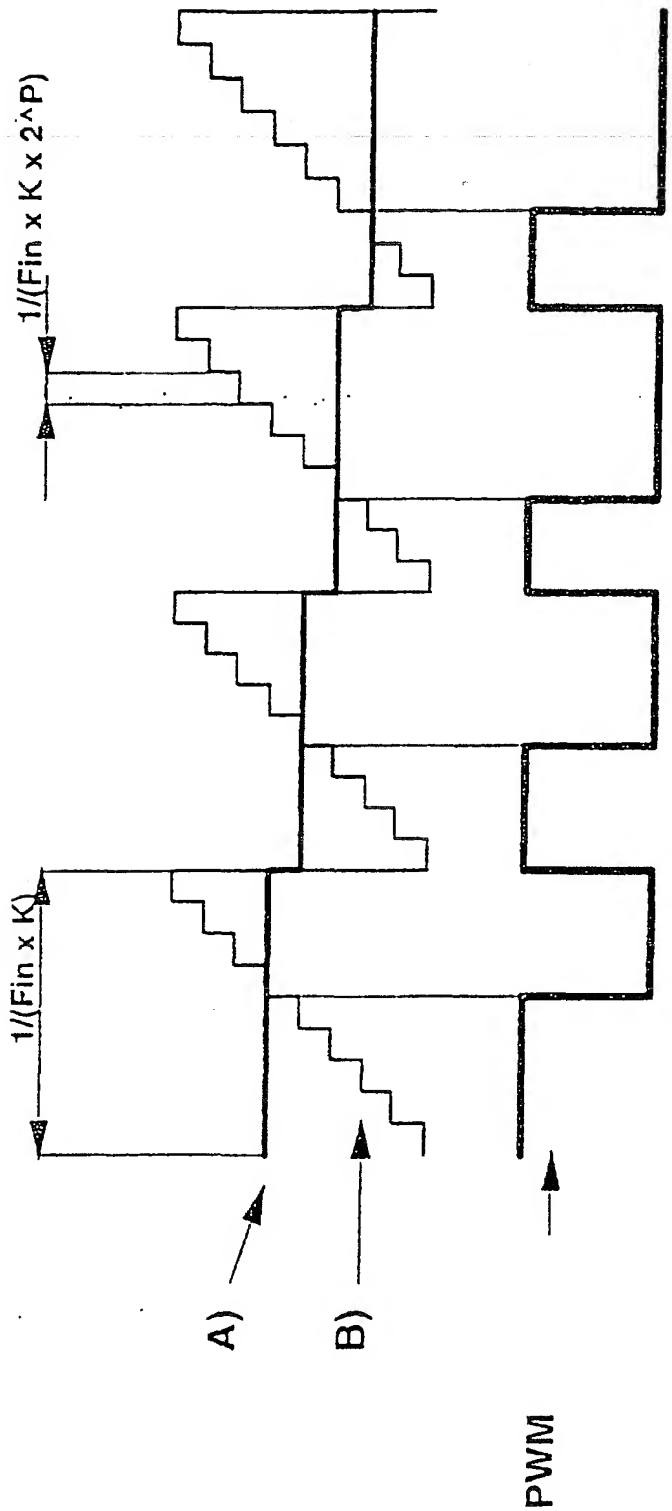

FIG. 4

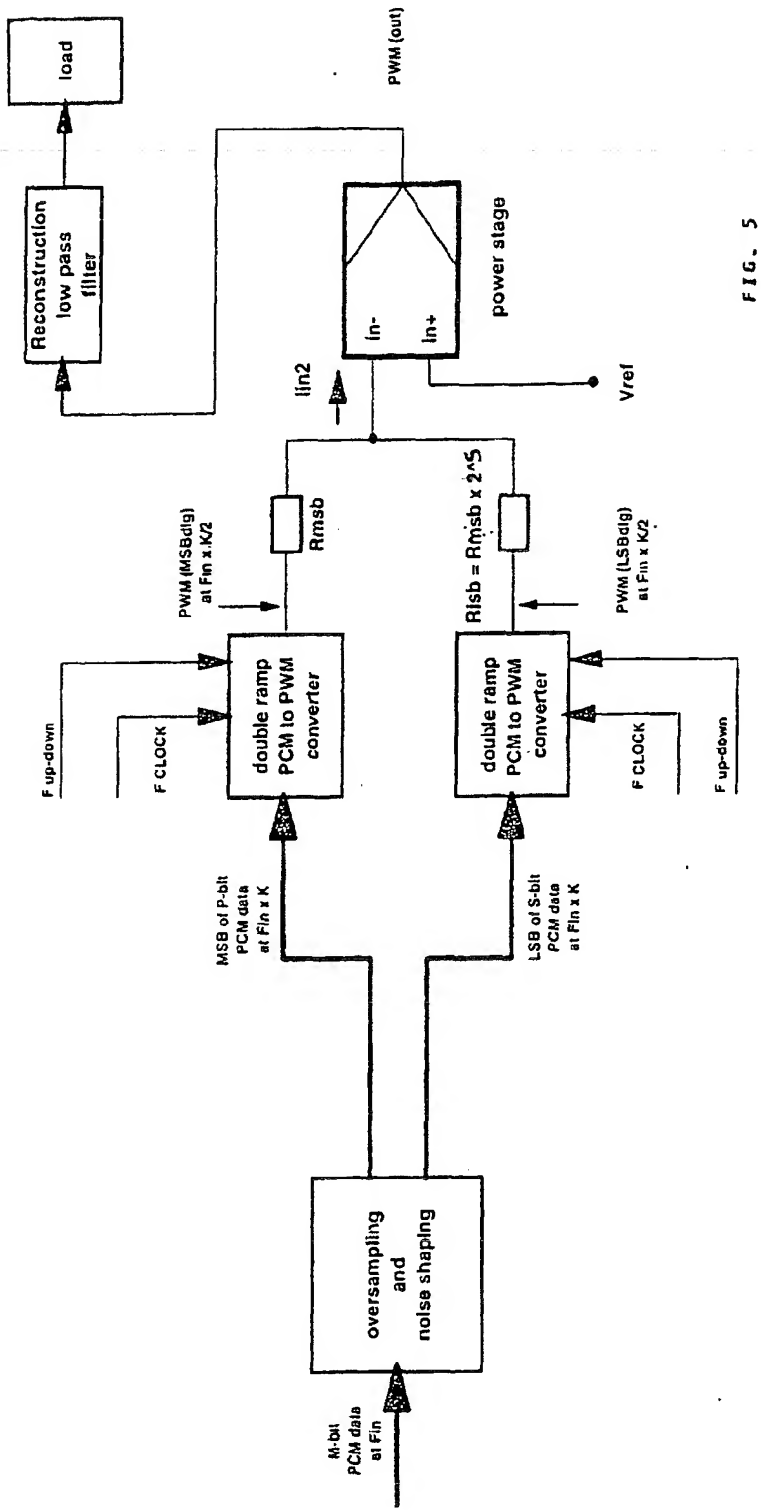
load
Reconstruction low pass filter
PWM (out)
power stage
in-
in+
Iin2
Vref
Rmsb
Rlsb = Rmsb x 2^5
PWM (MSBdig) at Fin x K/2
PWM (LSBdig) at Fin x K/2
double ramp PCM to PWM converter
double ramp PCM to PWM converter
F up-down
F CLOCK
F CLOCK
F up-down
MSB of P-bit PCM data at Fin x K
LSB of S-bit PCM data at Fin x K
oversampling and noise shaping
M-bit PCM data at Fin

FIG. 5

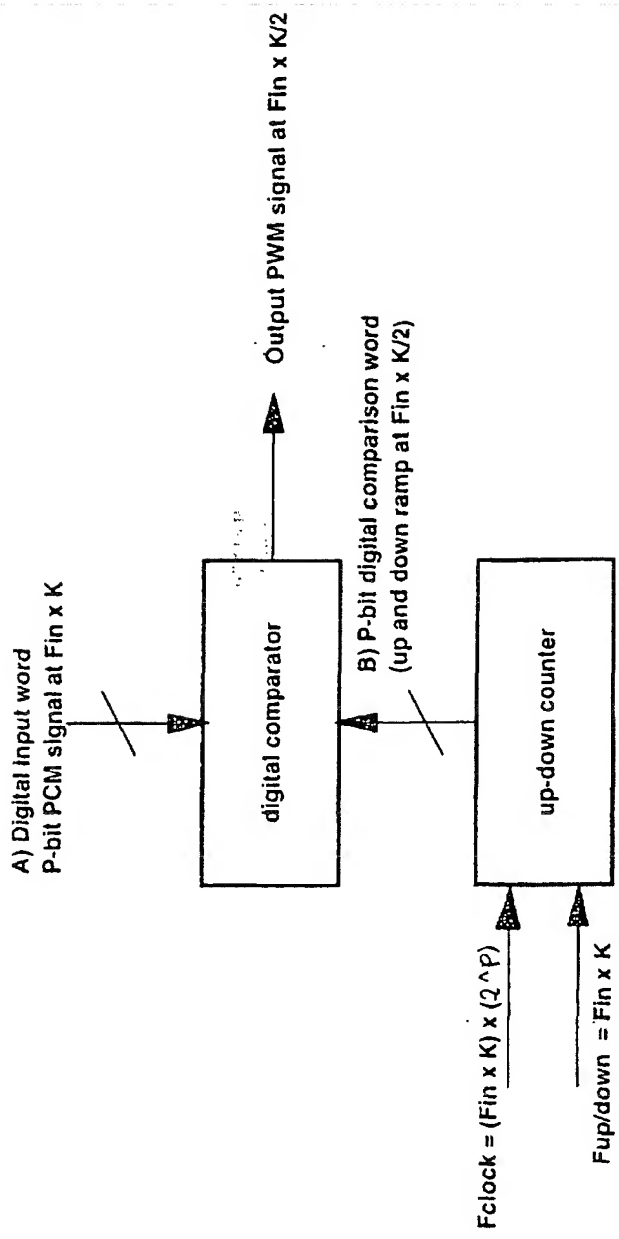
A) Digital input word
P-bit PCM signal at Fin x K
digital comparator
Output PWM signal at Fin x K/2
B) P-bit digital comparison word
(up and down ramp at Fin x K/2)
up-down counter
Fclock = (Fin x K) x (2^P)
Fup/down = Fin x K

FIG. 6

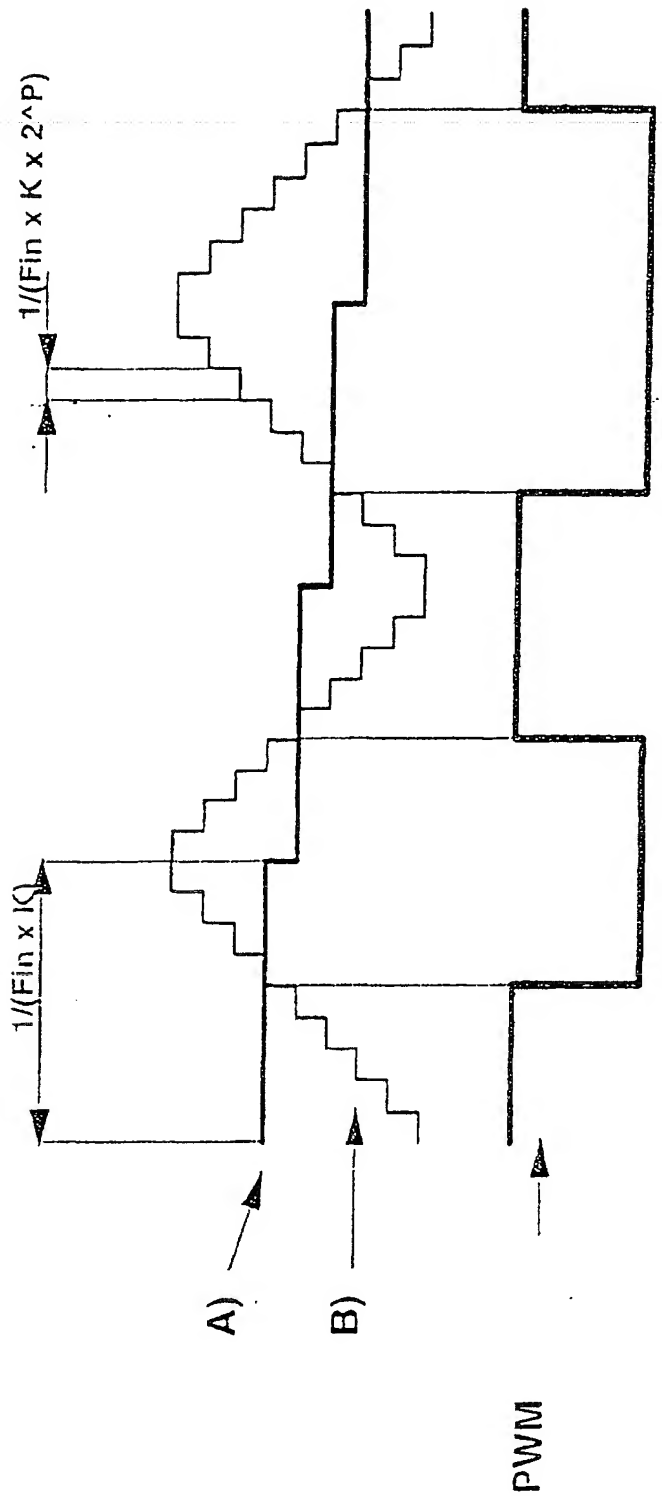

FIG. 7

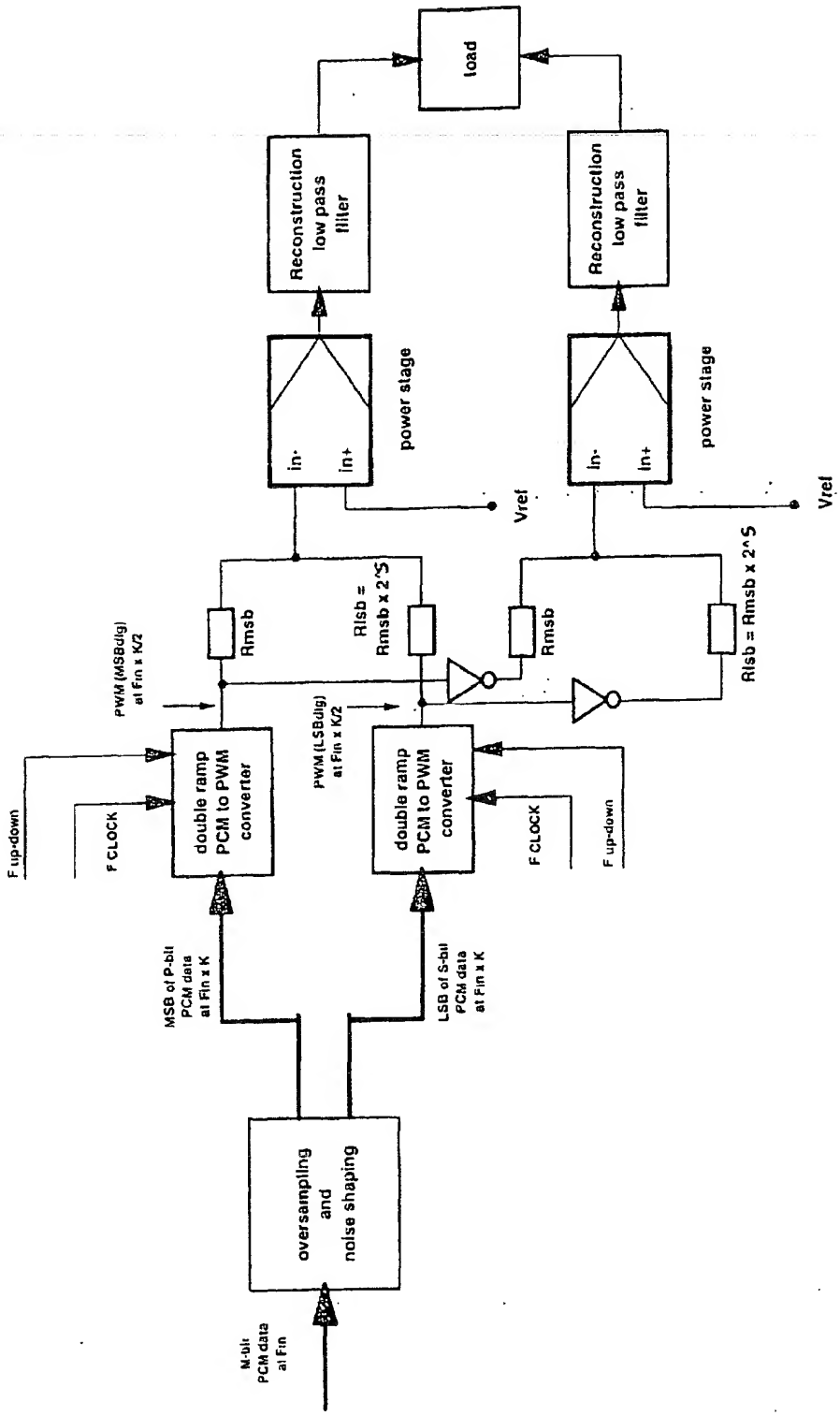
load
Reconstruction low pass filter
Reconstruction low pass filter
power stage
in-
in+
power stage
in-
in+
Vref
Vref
Rmsb
Rlsb = Rmsb x 2^S
Rmsb
Rlsb = Rmsb x 2^S
PWM (MSBdig) at Fin x K/2
PWM (LSBdig) at Fin x K/2
F up-down
F CLOCK
double ramp PCM to PWM converter
double ramp PCM to PWM converter
F CLOCK
F up-down
MSB of P-bit PCM data at Fin x K
LSB of S-bit PCM data at Fin x K
oversampling and noise shaping
M-bit PCM data at Fin

FIG. 8

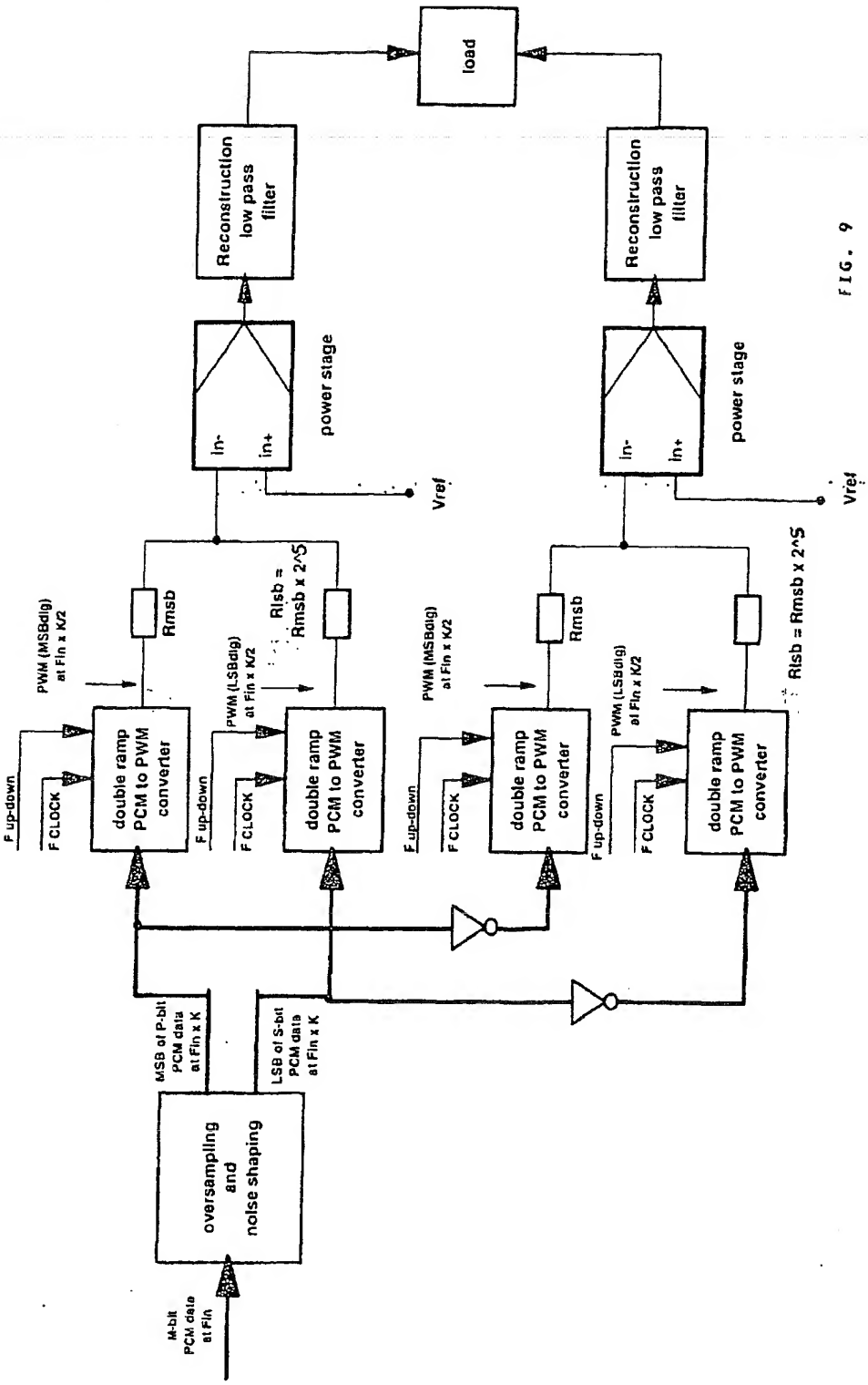
load
Reconstruction low pass filter
Reconstruction low pass filter
power stage
power stage
in-
in+
in-
in+
Vref
Vref
Rmsb
Rmsb
Rlsb = Rmsb x 2^5
Rlsb = Rmsb x 2^5
PWM (MSBdig) at Fin x K/2
PWM (LSBdig) at Fin x K/2
PWM (MSBdig) at Fin x K/2
PWM (LSBdig) at Fin x K/2
F up-down
F CLOCK
F up-down
F CLOCK
F up-down
F CLOCK
F up-down
F CLOCK
double ramp PCM to PWM converter
double ramp PCM to PWM converter
double ramp PCM to PWM converter
double ramp PCM to PWM converter
MSB of P-bit PCM data at Fin x K
LSB of S-bit PCM data at Fin x K
oversampling and noise shaping
M-bit PCM data at Fin

FIG. 9

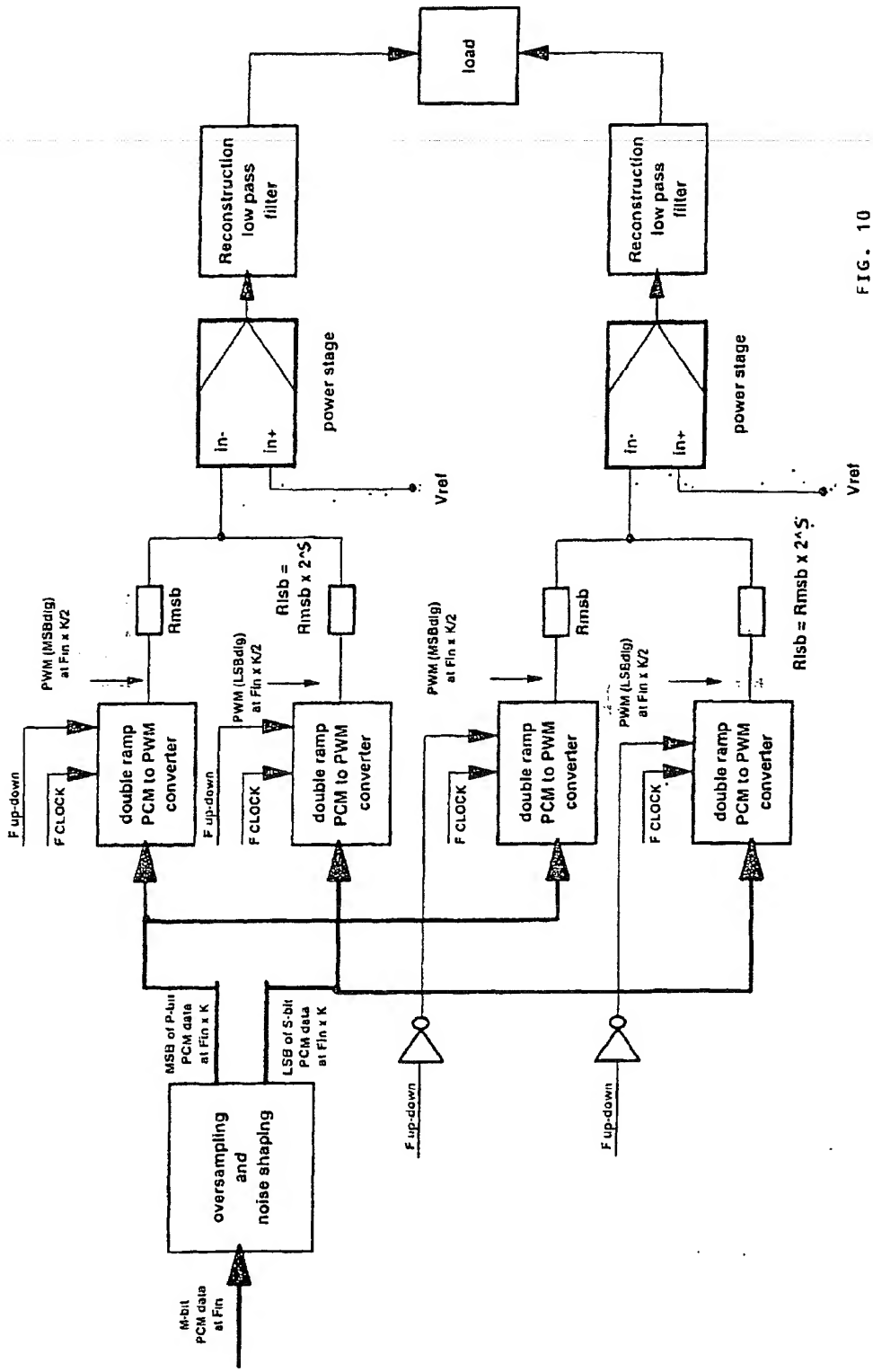
load
Reconstruction low pass filter
Reconstruction low pass filter
power stage
in-
in+
power stage
in-
in+
Vref
Vref
Rmsb
Rlsb = Rmsb x 2^S
Rmsb
Rlsb = Rmsb x 2^S
PWM (MSBdlg) at Fin x K/2
PWM (LSBdlg) at Fin x K/2
PWM (MSBdlg) at Fin x K/2
PWM (LSBdlg) at Fin x K/2
F up-down
F CLOCK
double ramp PCM to PWM converter
F up-down
F CLOCK
double ramp PCM to PWM converter
F CLOCK
double ramp PCM to PWM converter
F CLOCK
double ramp PCM to PWM converter
MSB of P-bit PCM data at Fin x K
LSB of S-bit PCM data at Fin x K
F up-down
F up-down
oversampling and noise shaping
M-bit PCM data at Fin

FIG. 10

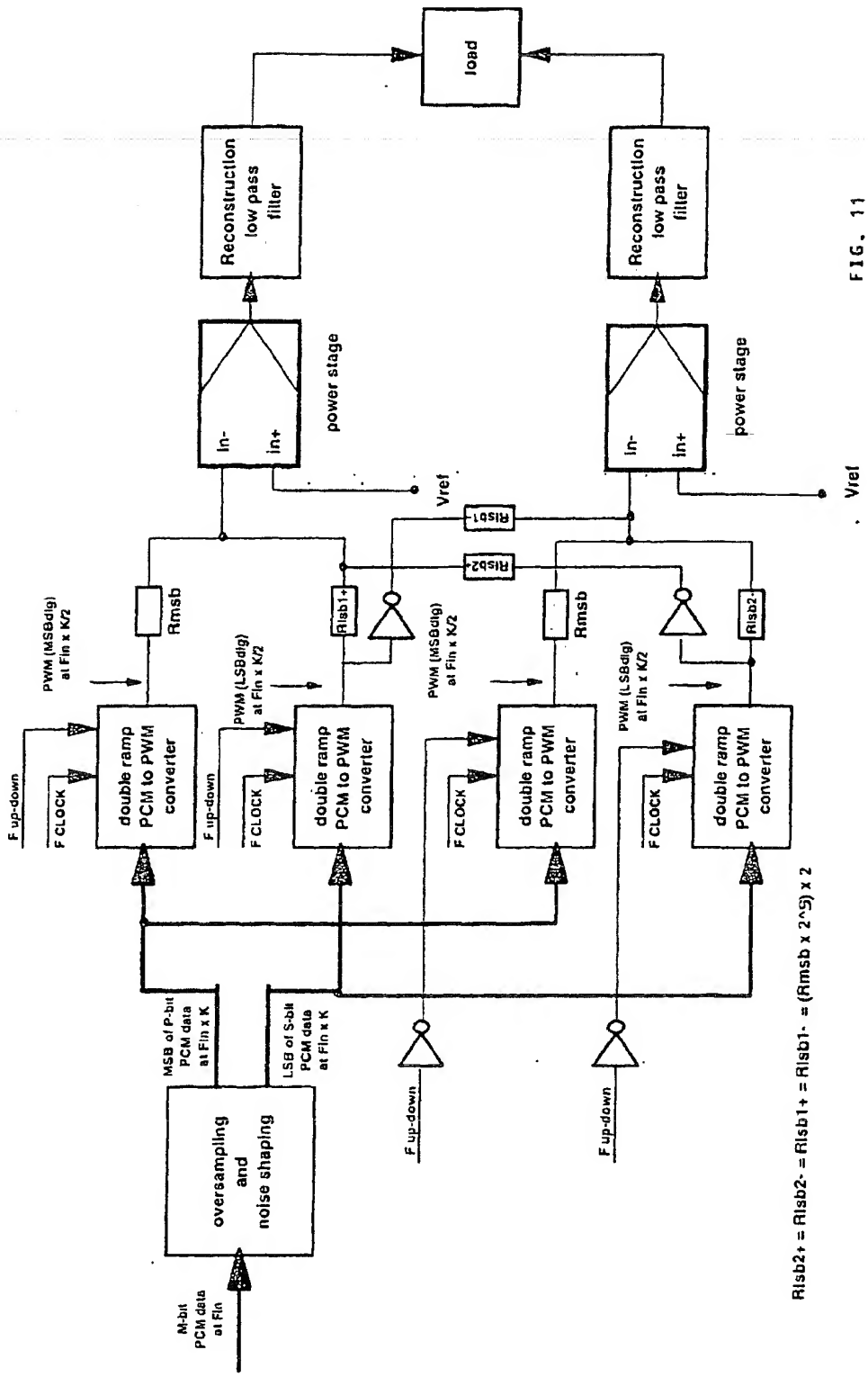
load
Reconstruction low pass filter
Reconstruction low pass filter
power stage
power stage
in-
in+
in-
in+
Vref
Vref
Rlsb1-
Rlsb2+
Rmsb
Rmsb
Rlsb1+
Rlsb2-
PWM (MSBdig) at Fin x K/2
PWM (LSBdig) at Fin x K/2
PWM (MSBdig) at Fin x K/2
PWM (LSBdig) at Fin x K/2
F up-down
F CLOCK
double ramp PCM to PWM converter
double ramp PCM to PWM converter
double ramp PCM to PWM converter
double ramp PCM to PWM converter
MSB of P-bit PCM data at Fin x K
LSB of S-bit PCM data at Fin x K
oversampling and noise shaping
M-bit PCM data at Fin
F up-down
F up-down
Rlsb2+ = Rlsb2- = Rlsb1+ = Rlsb1- = (Rmsb x 2^S) x 2

FIG. 11

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European Patent Office
Office européen des brevets

(11) EP 1 178 388 B1

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H03M 1/68 *(2006.01)* *H03M 1/82* *(2006.01)*

(21) Application number: **00830560.9**

(22) Date of filing: **04.08.2000**

(54) **PCM/PWM converter with PWM power amplifier**

Pulscodemodulation/Pulsbreitenmodulation-Umsetzer mit Pulsbreitenmodulation-Leistungsverstärker

Convertisseur MIC/MID avec amplificateur MID de puissance

(84) Designated Contracting States:
DE FR GB IT

(43) Date of publication of application:
06.02.2002 Bulletin 2002/06

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(56) References cited:
EP-A- 0 457 496
EP-A- 0 711 036
WO-A-00/35095
US-A- 6 066 988

EP 1 178 388 B1

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Description

[0001] The present invention is a PWM power ampliuci, specifically a digital input PWM power amplifier.

[0002] The general trend to reduce energy consumption and the weight and overall dimension represented by heatsinks has stimulated the request of equipment manufacturers for audio power amplifiers with greater efficiency than "AB" class amplifiers.

[0003] To meet these requests audio amplifiers in class D have been proposed which comprises a DC-AC converter circuit which produces a pulse width modulated (PWM) output signal; said PWM signal in turn drives power switches which drive a load provided with a passive filter for the reconstruction of the amplified audio signal.

[0004] A single output amplifier with analogue input and PWM output (class-D amplifier) is described in the article "Analysis of a quality class-D amplifier", F.A. Himmelstoss, et al., I.E.E.E. Transactions on Consumer Electronics, Vol. 42, No. 3, August 1996.

[0005] Widening interest in the digital processing of signals has lead to the manufacture of power amplifiers with digital input instead of analogue input. Said digital input power amplifiers include PCM/PWM converters capable of converting a PCM digital signal into a PWM digital signal, a final stage of power amplification receiving the PWM digital signal and generating an amplified PWM analogue output signal that drives a load provided with a passive filter for the reconstruction of the amplified audio signal. The PCM/PWM converter comprises a counter fed by a clock signal and generating digital comparison words and a digital comparator receiving the digital comparison words through a first input and the PCM digital signal through a second input and producing a digital PWM signal in output.

[0006] In a power amplifier of the above type, the device for generating the clock signal needed for the PCM/PWM conversion of the digital signal in input is typically made up of a PLL clock generator (phase locked) which, in per se known way, consists of a loop structure comprising a phase comparator, a filter, a volume controlled oscillator, a frequency divider.

[0007] A PLL clock generator nevertheless presents a complex structure and is affected by various types of noise above all in virtue of the presence of the phase comparator.

[0008] WO 0035095 discloses a digital-to-analog converter for converting M-bit digital input value into an analog output signal by separately processing the (M-N) number of most significant bits and the N number of least significant bits of the M-bit digital input values.

[0009] US 6066988 discloses a phase locked loop circuit including a reset signal generating circuit for generating a reference clock signal and a reset signal from an input clock signal.

[0010] EP 711036 discloses a variable delay circuit comprising a high speed clock generator receiving a trigger signal and outputting a pulse signal after a desired time interval from rising of the trigger signal and a coarse delay signal generator.

[0011] EP 457496 discloses a digital-to-analog converter suitable for a pulse width modulation system for converting input digital data into PWM signals and finally into an analog signal. The converter comprises PWM signal generation means which divides the sampling period of the digital data signal into a number m of sampling periods and which generates a PUN4 signal with two equal pulse widths corresponding to said input digital data in each divided sampling period.

[0012] In view of the state of the technique described, the object of the present invention is to present a PWM power amplifier provided with a clock generator that at least partially eliminates the above mentioned inconveniences.

[0013] In accordance with the present invention, said object is reached by means of a PWM power amplifier as defined in claim 1.

[0014] Thanks to the present invention a PWM power amplifier can be produced provided with a clock generator which has a simpler circuit than the known clock generator devices and which is less effected by noise in comparison with the same known devices.

[0015] The characteristics and advantages of the present invention will appear evident from the following detailed description of embodiments thereof, illustrated as non-limiting examples in the enclosed drawings, in which:

Figure 1 is a block diagram of the basic structure of the PWM power amplifier according to a first embodiment of the present invention;

Figure 2 is a block diagram of the clock generator of the power amplifier in figure 1;

Figure 3 shows the waveforms of the clock generator in Figure 2;

Figure 4 is a circuit diagram of the oscillator of the clock generator in Figure 2;

Figure 5 is a diagram of the internal structure of each of the two PCM/PWM single ramp converters in Figure 1;

Figure 6 shows the operating waveforms of a PCM/PWM single ramp converter;

Figure 7 is a block diagram of the basic structure of a power amplifier according to a second embodiment of the invention characterized by the use of PCM/PWM double ramp converters;

Figure 8 shows the internal structure of a PCM/PWM double ramp converter;

Figure 9 shows the operating waveforms of the PCM/PWM double ramp converter in Figure 8;

Figure 10 is a block diagram of the basic structure of a power amplifier according to a third embodiment of the invention;

Figure 11 is a block diagram of the basic structure of a power amplifier according to a fourth embodiment of the invention;

Figure 12 is a block diagram of the basic structure of a power amplifier according to a fifth embodiment of the invention;

Figure 13 is a block diagram of the basic structure of a power amplifier according to a sixth embodiment of the invention.

[0016] With reference to Figure 1 a power amplifier according to the first embodiment of the present invention is shown, in which initially a digital signal In with pulse code modulation (PCM) with a number M of bits at bit frequency Fin is sent in input to a block 1, where it is converted with oversampling techniques and noise shaping into a digital signal with a number N of bits lower than the number of bits of the digital signal In (M>N) and with a multiple bit frequency, Fin*k, compared to the bit frequency Fin of the digital signal In.

[0017] The N bits that compose the signal in output from the block 1 of oversampling and noise shaping are subdivided into two distinct buses, a first bus that transmits a first number P of more significant bits (MSB) and a second bus transmitting a number S of less significant bits (LSB), so as to form respective digital signals Ip and Is at the frequency Fin*k.

[0018] The digital signals Ip and Is are sent in input to two PCM/PWM converters, respectively the digital signal Ip is in input to the PCM/PWM converter 2 while the digital signal Is is in input to the PCM/PWM converter 3. The PCM/PWM converters 2 and 3 are part of a block 4 of conversion of digital data at pulse code modulation (PCM) into digital data at pulse width modulation (PWM) which also comprises a clock generator 5 suitable for producing a signal E at clock frequency Fclock necessary for the PCM/PWM conversion of the digital data.

[0019] The subdivision of the bits of the N bit digital signals into which the PCM digital signals in input In at M bit are reorganized, enables the use of not exceedingly high clock frequencies Fclock in the block 4. In fact, wanting to transform into a PWM signal a PCM signal at 16 bits at 44.1kHz without a noticeable deterioration of the signal/noise ratio, a sampling clock equal to $44100*2^{16}$=2.8GHz would be necessary, which is a value that could not be proposed for the present integrated circuits.

[0020] Another problem overcome by the subdivision carried out consists in the fact that the commutation frequency of the PWM signal in output, which in the example taken into consideration is 44.1kHz, would be too close to the maximum frequency to reproduce (generally in an audio system at about 20kHz), causing problems of harmonic distortion, frequency linearity and signal residues at commutation frequency downstream from the low-pass reconstruction filter.

[0021] If a commutation frequency of the PWM signal is required far enough from the audio band and considering the fact that normally the commutation frequency of the PWM amplifiers is between 100kHz and 500kHz, for example in the case considered about 44100*8=352.8kHz, and opting for a number of more significant bits (MSB) P=6 and a number of less significant bits (LSB) S=6, the clock frequency Fclock will be $352800*2^6$=22.57MHz, which can be handled with the present technologies used for the manufacture of integrated circuits.

[0022] The clock generator 5 comprises a reset pulse generator 6 and an oscillator 7, as can be seen in Figure 2. The reset pulse generator 6, which can be formed for example by a one-shot multivibrator, has a square wave IG input signal at frequency Fin*k, and generates an IR pulse output signal where the pulses are generated at each variation of the IG signal, as can be seen Figure 3. The signal IR is sent to an input R of the oscillator 7 which produces in output (OUT) the required clock signal E at frequency Fclock.

[0023] In Figure 4 a possible implementation of the oscillator 7 is shown. The input R of the oscillator 7 is placed on the gate terminal of a MOS transistor Mr which has the source grounded and the drain connected to a terminal of a capacitor C1 having the other terminal grounded, to the gate terminals of the MOS transistors M1, M2 being part of a first inverter, to the output OUT of the oscillator 7. The transistors M1, M2 have the source terminals connected to suitable current generators and the drain terminals connected to a terminal of a capacitor C2 which has the other terminal grounded and connected to the gate terminals of two MOS transistors M3, M4 being part of a second inverter. The transistors M3, M4 have the source terminals connected to suitable current generators and the drain terminals connected to a terminal of a capacitor C3 which has the other terminal grounded and connected to the gate terminals of two MOS transistors M5, M6 being part of a third inverter. The transistors M5, M6 have the source terminals connected to suitable current generators and the drain terminals connected to the output OUT. The bulk terminals of the transistors Mr, M2, M4, M6 are grounded while the bulk terminals of the transistors M1, M3, M5 are connected to a voltage supply Vcc. The transistor Mr brings the clock signal E at frequency Fclock to a low value when an impulse IR is present on its gate terminal, as can be seen in Figure 3; in this manner the oscillator 7 can be reset.

[0024] The functional block diagram and the functional waveforms valid for each of the two PCM/PWM converters 2 and 3 used in the PWM power amplifier in Figure 1 are shown in Figures 5 and 6; for simplicity only the PCM/PWM converter 2 will be described hereinafter.

[0025] Said PCM/PWM converter 2 is of the single ramp B type obtained by means of an up-counter, cyclic or resettable, powered by the clock signal E at frequency $Fclock=(Fin*k)*2^P$, that is equal to the product of the frequency of the signal Ip in input to the converter 2 by the power in base two of the number of bits P which form the signal Ip; the clock signal E is obtained by means of the clock generator 5 previously described. The ramp B signal is compared with the PCM digital signal Ip by a digital comparator 8; the result of the comparison is the PWM

digital signal Op in output from the converter 2 whose duty-cycle is function of the MSB input data and whose frequency is Fin*k. In the same manner the PWM digital signal Os in output from the converter 3 will have a duty-cycle which depends on the LSB input data and whose frequency is Fin*k.

[0026] The PWM digital signal Os in output from the converter 3 is attenuated in the block 9 by a ratio equivalent to the power in base two of the number S of bits transmitted to the input of the same converter thereby obtaining a signal O's=Os/(2^s). The signals Op and O's are summed at the inverting node of a power amplification final block 10 (the output stage of the PWM power amplifier) which is the power amplification module functioning in class D described and illustrated in the European patent application No. 1001526. A reference voltage Vref is connected to the non-inverting node of the block 10.

[0027] The PWM digital signal Op produced by the PCM/PWM converter 2 drives the output stage 10 determining its commutation frequency. The PWM digital signal O's drives the block 10 with a weight reduced by $1/2^s$; in this manner the signal O's modulates the PWM signal Iout in output from block 10 correcting its non-linearity and attenuating the noise introduced by the quantization to a reduced number P of bits of the PWM digital signal Op.

[0028] The amplified PWM signal Iout is sent in input to a low-pass filter 11 which provides for the reconstruction of the starting audio signal; the signal in output from filter 11 will be sent to a load 12 made up for example by a loudspeaker.

[0029] Hereinafter other embodiments of the present invention will be described in which the elements equal to the first or to other embodiments will have the same references.

[0030] In Figures 7-9 a PWM power amplifier according to a second embodiment is described which differs from the first embodiment in the use of the PCM/PWM double ramp converters instead of single ramp converters; in this manner the frequency of the PWM signals produced in output from the two PCM/PWM 2 and 3 converters is halved compared to the Fin*k frequency of the digital signals Ip an Is in input to the converters 2 and 3.

[0031] The functional block diagram and the functional waveforms valid for each of the two PCM/PWM double ramp converters 2 and 3 used in the PWM power amplifier in Figure 1 are shown in Figures 8 and 9; for simplification only the PCM/PWM converter 2 will be described hereinafter.

[0032] Said PCM/PWM converter 2 is of the double ramp Z type obtained by means of an up-down counter, cyclic or resettable, powered both with the signal of clock E at frequency Fclock=(Fin*k)*2^P, that is equal to the product of the frequency of the signal Ip in input to the converter 2 by the power in base two of the number of bits P that form the signal Ip (the clock signal E is obtained by means of the clock generator 5 previously described), and with a second clock signal D at frequency Fup/down (produced by a clock generator different from generator 5) with the frequency Fup/down=Fin*k which synchronizes the ramp inversions. The double ramp signal Z is compared with the PCM digital signal Ip by a digital comparator 8; the result of the comparison is the PWM digital signal Op in output from converter 2 whose duty-cycle is function of the MSB input data and whose frequency is Fin*k/2. In the same manner the PWM digital signal Os in output from converter 3 will have a duty-cycle which depends on the LSB input data and whose frequency is Fin*k/2.

[0033] The PWM digital signal Os in output from converter 3 is attenuated in block 9 in a ratio equivalent to the power in base two of the number S of bits transmitted to the input of the sane converter obtaining a signal O's=Os/(2^s). The signals Op and O's are summed at the inverting node of the power amplification final block 10.

[0034] The double ramp converters enable the performance of the amplifier to be improved from the point of view of the signal/noise ratio and of the distortion compared to the use of single ramp converters.

[0035] The block diagram of a PWM power amplifier according to a third embodiment of the invention is shown in Figure 10, differing from the second embodiment previously described only in the presence of an output which is no longer single but of bridge type, using two push-pull driven output stages 101 and 102 (with relative low-pass filters 111 and 112). The signals Op and O's are summed at the inverting node of the first output stage 101 while the signals Opn and O'sn (the signal O'sn is the signal Osn attenuated by block 9), which are respectively signals Op and O's negated, are summed at the inverting node of the output second stage 102. The output signals of the two stages 101 and 102 I'out and I"out are sent to the respective low-pass filters 111 and 112 and the output signals of the filters drive the load 12.

[0036] Figure 11 shows the block diagram of a PWM power amplifier according to a fourth embodiment of the invention which differentiates from the third embodiment previously described in that it provides for a double ramp conversion both for the signals Ip and Is and for the signals Ipn and Isn, which are the signals Ip and Is negated, by means of further double ramp PCM/PWM converters 20 and 30, similar to the converters 2 e 3, which supply in output the signals Opn and Osn. In said case the output of the PWM power amplifier is of the phase shift bridge type and presents a more complex architecture than that in Figure 10 but is capable of giving higher performance, as is described in detail and illustrated in the European patent application No. 1001526

[0037] Figure 12 shows the block diagram of a PWM power amplifier according to a fifth embodiment of the invention which differentiates from the fourth embodiment previously described in that the signals Opn and Osn in output from the PCM/PWM converters 20 and 30 derive not from inverted digital signals Ipn and Isn but by inverting the clock signal D at frequency Fup/down of the up-down counters of the converters 20 and 30, such as

to generate triangular signals in counter-phase between each other.

[0038] Figure 13 shows the block diagram of a PWM power amplifier according to a sixth embodiment of the invention which differentiates from the fifth embodiment previously described because the PWM digital signals Op and Opn are summed to twice the respective signals O's1 and O'sn1 which are the signals O's and O'sn at double frequency compared to the frequency of the signals Op and Opn, at the respective inverting nodes of the two output stages 101 and 102.

[0039] The advantages of said embodiment lie both in the fact that the correction signal (relative to the signals Os and Osn) can be added, subtracted or can also not influence the main drive signal (relative to the signals Op and Opn), and in the fact that the correction signal does not contain tones at PWM commutation frequency or in its proximity (the tones of a band of 20kHz around a commutation frequency are returned to base band causing an increase in distortion or noise).

[0040] In the embodiments illustrated in the Figures the blocks 9 and 200 can be constituted by simple resistors or by current generators controlled by the output logic signal of the respective PCM/PWM converters.

[0041] The frequency of the oscillator 7 of the clock generator 5 can be varied by continuously changing its characteristics; the consequence is a continuous variation of the width of the output signal of the PWM amplifier due to the variable gain of the PCM/PWM conversion block 4.

[0042] In all the embodiments previously described the clock signal E at frequency Fclock is produced by the generator 5 of Figure 2.

Claims

1. PWM power amplifier comprising at least one PCM/PWM converter (2, 3, 20, 30) which is fed by PCM digital input signals (Ip, Is) and produces PWM digital output signals (Op, Os, Opn, Ops), and at least one final stage (10, 101, 102) of power amplification of the PWM digital signals (Op, Os, Opn, Ops) in output from said at least one PCM/PWM converter (2, 3, 20, 30), said at least one PCM/PWM converter (2, 3, 20, 30) comprising a up-counter or up-down counter fed with at least one clock signal (E) produced by a clock generator device (5) and comprising a digital comparator (8) suitable for comparing said PCM digital input signals (Ip, Is) of said at least one PCM/PWM converter (2, 3, 20, 30) with a digital comparison signal (B, Z) produced by said up-counter or up-down counter and producing in output said digital signals PWM (Op, Os, Opn, Ops), **characterized in that** said clock generator device (5) comprises a pulse generator device (6) and an oscillator (7), said pulse generator device (6) receiving a signal at a frequency (Fin*k) equal to the frequency of said PCM digital input signals (Ip, Is) of said at least one PCM/PWM converter (2, 3, 20, 30) and producing output reset pulses (IR), said reset pulses (IR) being sent to the input of said oscillator (7) producing as output said at least one clock signal (E).

2. Amplifier according to claim 1, **characterized in that** it comprises an oversampling and noise shaping block (1) receiving first PCM digital input signals (In) organized in words with a given number of bits (M) and at a given frequency (Fin) and producing as output second PCM digital signals (Ip, Is) organized in words composed of a number of bits (N) lower than said given number of bits (M) and at a multiple frequency (Fin*k) with respect to said given frequency (Fin) of the first PCM digital input signals (In), said second PCM digital signals (Ip, Is) being the PCM digital signals in input to said at least one PCM/PWM converter (2, 3, 20, 30).

3. Amplifier according to claim 2, **characterized in that** it comprises a first bus suitable for transmitting first digital data PCM (Ip) containing a first number (P) of more significant bits (MSB) of said second PCM digital signals (Ip, Is) and a second bus suitable for transmitting second PCM digital data (Is) containing a second number (S) of less significant bits (LSB) of said second PCM digital signals (Ip, Is), and **characterized in that** it foresees a first (2, 20) and a second (3, 30) PCM/PWM converter fed respectively by said first (Ip) and second (Is) PCM digital data and producing in output respectively a first (Op, Opn) and a second (Os, Osn) PWM signal.

4. Amplifier according to claim 3, **characterized in that** said second signal PWM (Os, Osn) is previously attenuated by a ratio equivalent to the power in base two of the second number (S) of less significant bits (LSB) transmitted by said second bus to the input of said second PCM/PWM converter (3, 30) and is summed to said first signal PWM (Op, Opn) at an inverting node (-) of said at least one power amplification final stage (10, 101, 102) of the amplifier.

5. Amplifier according to claim 1, **characterized in that** said at least one clock generator (5) produces a clock signal (E) whose frequency (Fclock) equals the product of the frequency (Fin*k) of the bits of the PCM digital signals (Ip, Is) as input to said at least one PCM/PWM converter (2, 3, 20, 30) by the power of base two of the number of bits (P, S) of said PCM digital signals (Ip, Is) being input to at least one PCM/PWM converter (2, 3, 20, 30), said up-counter or up-down counter fed by said at least one clock signal (E) generating a digital comparison output signal (B, Z) composed of said number of bits (P, S) in the form of at least one ramp of digital values at an identical or halved frequency compared to said fre-

quency (Fin*k) of bits of the PCM digital signals (Ip, Is) in input to the at least one PCM/PWM converter (2, 3, 20, 30).

6. Amplifier according to claim 5, **characterized in that** said digital comparison signal (B) of said at least one PCM/PWM converter (2, 3, 20, 30) is in the form of a succession of upward ramps of digital values at a frequency identical to said frequency (Fin*k) of bits of the PCM digital signals (Ip, Is) being input to at least one PCM/PWM converter (2, 3, 20, 30).

7. Amplifier according to claim 5, **characterized in that** said at least one PCM/PWM converter (2, 3, 20, 30) is a double ramp type, said (up-down counter being of the up/down type, having as input a ramp inversion signal (D) and generating as output a digital comparison signal (Z) composed by the number of bits (P, S) of said PCM digital signals (Ip, Is) being input to at least one PCM/PWM converter (2, 3, 20, 30) under the form of a succession of up and down ramps at a halved frequency (Fin*k/2) compared to the frequency of the PCM digital signals (Ip, Is) being input to said at least one PCM/PWM converter (2, 3, 20, 30).

8. Amplifier according to the claims 1 or 4, **characterized in that** it foresees a single power amplification final stage (10).

9. Amplifier according to the claims 1 or 4, **characterized in that** it foresees two identical power amplification final stages (102, 102) functioning in counterphase and in which the inversion of the signal fed to the inverting input of said two final stages is made by inverting the PWM digital signal (Op, Os) being output from said at least one PCM/PWM converter (2, 3).

10. Amplifier according to the claims 1 or 4, **characterized in that** it foresees two identical power amplification final stages (101, 102) functioning in counterphase and in which the inversion of the signal fed to the inverting input (-) of said two final stages (101, 102) is made by duplicating said at least one PCM/PWM converter (2, 3) and inverting the PCM digital signals (Ip, Is) being input to said at least two PCM/PWM converters (2, 3).

11. Amplifier according to the claims 1 and 4, **characterized in that** said at least one clock generator (5) produces a clock signal (E) whose frequency (Fclock) equals the product of the frequency (Fin*k) of the bits of the PCM digital signals (Ip, Is) being input to said at least one PCM/PWM converter (2, 3, 20, 30) by the power of base two of the number of bits (P, S) of said PCM digital signals (Ip, Is) being input to at least one PCM/PWM converter (2, 3, 20, 30), said at least one PCM/PWM converter (2, 3, 20, 30) is a double ramp type, said up-down counter being fed by said clock signal (E) and being the up/down type, having as input a ramp inversion signal (D) and generating as output a digital comparison signal (Z) composed of the number of bits (P, S) of said PCM digital signals (Ip, Is) being input to at least one PCM/PWM converter (2, 3, 20, 30) in the form of a succession of up and down ramps at a halved frequency (Fin*k/2) compared to the frequency of the PCM digital signals (Ip, Is) being input to said at least one PCM/PWM converter (2, 3, 20, 30), and **characterized in that** it foresees two identical power amplification final stages (101, 102) functioning in counterphase and in which the inversion of the signal fed to the inverting input (-) of said two final stages (101, 012) is made by duplicating said at least one PCM/PWM double ramp converter (2, 3) and inverting the ramp inversion signal (D) of said at least one PCM/PWM converter (2, 3) and feeding both said at least one PCM/PWM converter (2, 3) and its duplicate (20, 30) with the same PCM input digital signals (Ip, Is).

12. Amplifier according to claim 4, **characterized in that** said at least one clock generator (5) produces a clock signal (E) whose frequency (Fclock) equals the product of the frequency (Fin*k) of the bits of the PCM digital signals (Ip, Is) in input to said at least one PCM/PWM converter (2, 3, 20, 30) by the power of base two of the number of bits (P, S) of said PCM digital signals (Ip, Is) being input to at least one PCM/PWM converter (2, 3, 20, 30), said at least one PCM/PWM converter (2, 3, 20, 30) being double ramp type, said up-down counter being fed by said clock signal (E) and being the up/down type, having as input a ramp inversion signal (D) and generating in output a digital comparison signal (Z) composed of the number of bits (P, S) of said PCM digital signals (Ip, Is) being input to at least one PCM/PWM converter (2, 3, 20, 30) in the form of a succession of up and down ramps at a halved frequency (Fin*k/2) compared to the frequency of the PCM digital signals (Ip, Is) being input to said at least one PCM/PWM converter (2, 3, 20, 30), and **characterized in that** it foresees two identical power amplification final stages (101, 102) functioning in counterphase and in which the inversion of the signal fed to the inverting input (-) of said two final stages (101, 102) is made by duplicating said couple of PCM/PWM double ramp converters (2, 3) and inverting the signal of ramp inversion (D) of said couple of PCM/PWM converters (2, 3) and feeding both said couple of PCM/PWM converters (2, 3) and their duplicate (20, 30) with the same PCM digital signals (Ip, Is) of said first bus and of said second bus.

13. Amplifier according to claim 12, **characterized in**

that it comprises means for inverting the PWM signals (Os, Osn) produced at the output of the PCM/PWM converters (3, 30) of said couple (2, 3) and its duplicate (20, 30) which are fed with said PCM digital signals (Is) containing the less significant bits (LSB), means for attenuating (200) the inverted PWM signals and means for summing each of said PWM signals inverted and attenuated on the inverting node (-) on which the PWM signals produced by the PCM/PWM converters (2, 20) belonging to the other one between said couple (2, 3) of converters or its duplicate (20, 30) are summed.

14. Amplifier according to claim 1, **characterized in that** said oscillator (7) comprises inverters each formed by a couple of MOS transistors (M1, M2; M3, M4; M5, M6) and placed in series and in a loop so that the input of the first of said inverters is connected with the output of the last of said inverters, capacities (C1, C2, C3) in a number equal to that of the inverters and each one having a terminal connected to a respective input of each inverter and the other terminal grounded, a transistor MOS (Mr) having as input said reset pulses (IR) and the output connected to the input of said first inverter.

Patentansprüche

1. PCM-Leistungsverstärker mit
zumindest einem PCM/PWM-Umsetzer (2, 3, 20, 30), der mit digitalen PCM-Eingangssignalen (Ip, Is) gespeist wird und digitale PWM-Ausgangssignale (Op, Os, Opn, Ops) erzeugt, und
zumindest einer Endstufe (10, 101, 102) der Leistungsverstärkung der digitalen PWM-Signale (Op, Os, Opn, Ops) am Ausgang des zumindest einen PCM/PWM-Umsetzers (2, 3, 20, 30),
wobei der zumindest eine PCM/PWM-Umsetzer (2, 3, 20, 30):

    einen Aufwärt.szähler oder einen Aufwärts/Abwärtszähler enthält, der mit zumindest einem Taktsignal (E) gespeist wird, das von einer Takterzeugungsvorrichtung (5) erzeugt wird, und einen digitalen Komparator (8) enthält, der geeignet ist, die digitalen PCM-Eingangssignale (Ip, Is) des zumindest einen PCM/PWM-Umsetzers (2, 3, 20, 30) mit einem digitalen Vergleichssignal (B, Z) zu vergleichen, das von dem Aufwärtszähler oder Aufwärts/Abwäztszähler erzeugt wurde, und am Ausgang die digitalen PWM-Signale (Op, Os, Opn, Ops) zu erzeugen;

dadurch gekennzeichnet, dass
die Taktexzeugungsvorrichtung (5) eine Pulserzeugungsvorrichtung (6) und einen Oszillator (7) enthält, die Pulserzeugungsvorrichtung (6) ein Signal mit einer Frequenz (Fin*k) gleich der Frequenz der digitalen PCM-Eingangssignale (Ip, Is) des zumindest einen PCM/PWM-Umsetzers (2, 3, 20, 30) empfängt und Ausgangsrücksetzpulse (IR) erzeugt, und
die Ausgangsrücksetzpulse (IR) an den Eingang des Oszillators (7) gesendet werden, der das zumindest einem Taktsignal (E) als Ausgabe erzeugt.

2. Verstärker nach Anspruch 1, **dadurch gekennzeichnet, dass** er einen Überabtast- und Rauschformblock (1) enthält, der ein erstes digitales PCM-Eingangssignal (In) empfängt, das in Wörtern mit einer vorgegebenen Anzahl von Bits (M) bei einer vorgegebenen Frequenz (Fin) organisiert ist, und als Ausgabe zweite digitale PCM-Signale (Ip, Is) erzeugt, die in Wörtern organisiert sind, die aus einer kleineren Anzahl von Bits (N) als die vorgegebene Anzahl von Bits (M) und mit einer Vielfachfrequenz (Fin*k) relativ zu der vorgegebenen Frequenz (Fin) des ersten digitalen PCM-Eingangssignals (In) zusammengesetzt sind,
wobei die zweiten digitalen PCM-Signale (Ip, Is) die digitalen PCM-Signale am Eingang des zumindest einen PCM/PWM-Umsetzers (2, 3, 20, 30) sind,

3. Verstärker nach Anspruch 2, **dadurch gekennzeichnet, dass** er enthält:

    einen ersten Bus, der geeignet ist, erste digitale PCM-Daten (Is) zu übertragen, die eine erste Anzahl (P) von höherwertigen Bits (MSB) der zweiten digitalen PCM-Signale (Ip, Is) enthalten, und
    einen zweiten Bus, der geeignet ist, zweite digitale PCM-Daten (Ip) zu übertragen, die eine zweite Anzahl (S) von niedrigerwertigen Bits (LSB) der zweiten digitalen PCM-Signale (Ip, Is) enthalten, und
    dadurch gekennzeichnet, dass er ein erster (2, 20) und ein zweiter (3, 30) PCM/PWM-Umsetzer vorgesehen sind, die jeweils von den ersten (Ip) bzw. den zweiten (Is) digitalen PCM-Daten gespeist werden und am Ausgang jeweils ein erstes (Op, Opn) und ein zweites (Os, Osn) PWM-Signal erzeugen.

4. Verstärker nach Anspruch 3, **dadurch gekennzeichnet, dass**
das zweite PWM-Signal (Os, Osn) vorher in einem Verhältnis gedämpft wird, das gleich der Potenz 2 hoch die zweite Anzahl (S) von niedrigerwertigen Bits (LSB) ist, die von dem zweiten Bus zu dem Eingang des zweiten PCM/PWM-Umsetzers (3, 30) übertragen werden, und
an einem invertierenden Knoten (-) der zumindest einen Leistungsverstärkungsendstufe (10, 101, 102) des Verstärkers zu dem ersten PWM-Signal (Op, Opn) addiert wird.

5. Verstärker nach Anspruch 1, **dadurch gekennzeichnet, dass**
der zumindest eine Taktgenerator (5) ein Taktsignal (E) erzeugt, dessen Frequenz (Fclock) gleich dem Produkt aus der Frequenz (Fin*k) der Bits der digitalen PCM-Signale (Ip, Is) als Eingabe für den zumindest einen PCM/PWM-Umsetzer (2, 3, 20, 30) und der Potenz 2 hoch die Anzahl der Bits (P, S) der digitalen PCM-Signale (Ip, Is) ist, die dem zumindest einen PCM/PNM-Umsetzer (2, 3, 20, 30) eingegeben werden,
wobei der Aufwärtszähler oder Aufwärts/Abwärtszähler, der von dem zumindest einen Taktsignal (E) gespeist wird, ein digitales Vergleichsausgabesignal (B, Z) erzeugt bestehend aus der Anzahl von Bits (P, S) in der Form zumindest einer Rampe von Digitalwerten mit derselben oder der halben Frequenz verglichen mit der Frequenz (Fin*k) der Bits der digitalen PCM-Signale (Ip, Is) am Eingang des zumindest einen PCM/PWM-Umsetzers (2, 3, 20, 30)

6. Verstärker nach Anspruch 5, **dadurch gekennzeichnet, dass** das digitale Vergleichssignal (B) des zumindest einen PCM/PWM-Umsetzers (2, 3, 20, 30) ausgebildet ist in der Form einer Aufeinanderfolge von Aufwärtsrampen von Digitalwerten mit einer Frequenz, die dieselbe ist wie die Frequenz (Fin*k) der Bits der digitalen PCM-Signale (Ip, Is), die dem zumindest einen PCM/PWM-Clmsetzex (2, 3, 20, 30) eingegeben werden

7. Verstärker nach Anspruch 5, **dadurch gekennzeichnet, dass**
der zumindest eine PCM/PWM-Umsetzer (2, 3, 20, 30) ein Doppelrampentyp ist,
der Aufwärts/Abwärtszähler vom Aufwärts/Abwärtstyp ist, als Eingabe ein Rampeninversionssignal (D) hat und als Ausgabe ein digitales Vergleichssignal (Z) erzeugt bestehend aus der Anzahl von Bits (P, S) der digitalen PCM-Signale (Ip, Is), die dem zumindest einen PCM/PWM-Umsetzer (2, 3, 20, 30) eingegeben werden, in der Form einer Aufeinanderfolge von Aufwärts- und Abwärtsrampen bei einer halben Frequenz (Fin*k/2) verglichen mit der Frequenz der digitalen PCM-Signale (Ip, Is), die dem zumindest einen PCM/PWM-Umsetzer (2, 3, 20, 30) eingegeben werden.

8. Verstärker nach Anspruch 1 oder 4, **dadurch gekennzeichnet, dass** eine einzige Leistungsverstäxkungsendstufe (10) vorgesehen ist.

9. Verstärker nach Anspruch 1 oder 4, **dadurch gekennzeichnet, dass** zwei identische Leistungsverstärkungsendstufen (101, 102) vorgesehen sind, die im Gegentakt arbeiten und bei denen das Invertieren des Signals, das dem invertierenden Eingang der zwei Endstufen zugeführt wird, geschieht durch Invertieren des digitalen PWM-Signals (Op, Os), das von dem zumindest einen PCM/PWM-Umsetzer (2, 3) ausgegeben wird,

10. Verstärker nach Anspruch 1 oder 4, **dadurch gekennzeichnet, dass** zwei identische Leistungsverstärkungsendstufen (101, 102) vorgesehen sind, die im Gegentakt arbeiten und bei denen das Invertieren des Signals, das dem invertierenden Eingang (-) der zwei Endstufen (101, 102) zugeführt wird, geschieht durch Verdoppeln des zumindest einen PCM/PWM--Umsetzer (2, 3) und Invertieren der digitalen PCM-Signale (Ip, Is), die dem zumindest einen PCM/PWM-Umsetzer (2, 3) eingegeben werden.

11. Verstärker nach Anspruch 1 und 4, **dadurch gekennzeichnet, dass**
der zumindest eine Taktgenerator (5) ein Taktsignal (E) erzeugt, dessen Frequenz (Fclock) gleich dem Produkt aus der Frequenz (Fin*k) der Bits der digitalen PCM-Signale (Ip, Is), die dem zumindest einen PCM/PWM-Umsetzer (2, 3, 20, 30) eingegeben werden, und der Potenz 2 hoch die Anzahl der Bits (P, S) der digitalen PCM-Signale (Ip, Is) ist, die dem zumindest einen PCM/PWM-Umsetzer (2, 3, 20, 30) eingegeben werden,
der zumindest eine PCM/PWM-Umsetzer (2, 3, 20, 30) ein Doppelrampentyp ist,
der Aufwärts/Abwärtszähler, der von dem Taktsignal (E) gespeist ist und vom Aufwärts/Abwärtstyp ist, als Eingabe ein Rampeninversionssignal (D) hat und als Ausgabe ein digitales Vergleichssignal (Z) erzeugt bestehend aus der Anzahl von Bits (P, S) der digitalen PCM-Signale (Ip, Is), die dem zumindest einen PCM/PWM-Umsetzer (2, 3, 20, 30) eingegeben werden, in der Form einer Aufeinanderfolge von Aufwärts- und Abwärtsrampen bei einer halben Frequenz (Fin*k/2) verglichen mit der Frequenz der digitalen PCM-Signale (Ip, Is), die dem zumindest einen PCM/PWM-Umsetzer (2, 3, 20, 30) eingegeben werden, und
dadurch gekennzeichnet, dass zwei identische Leistungsverstärkungsendst.ufen (101, A02) vorgesehen sind, die im Gegentakt arbeiten und bei denen das Invertieren des Signals, das dem invertierenden Eingang (-) der zwei Endstufen (101, 102) zugeführt wird, geschieht durch Verdoppeln des zumindest einen PCM/PWM-Doppelrampenumsetzers (2, 3) und Invertieren des Rampeninversionssignals (D) des zumindest einen PCM/PWM-Umsetzers (2, 3) und Speisen sowohl des zumindest einen PCM/PWM-Umsetzers (2, 3) als auch seines Duplikats (20, 30) mit denselben digitalen PCM-Signalen (Ip, Is).

12. Verstärker nach Anspruch 4, **dadurch gekennzeichnet, dass**
der zumindest eine Taktgenerator (5) ein Taktsignal (E) erzeugt, dessen Frequenz (Fclock) gleich dem

Produkt aus der Frequenz (Fin*k) der Bits des digitalen PCM-Signals (Ip, Is) am Eingang des zumindest einen PCM/PWM-Umsetzers (2, 3, 20, 30) und der Potenz 2 hoch die Anzahl der Bits (P, S) der digitalen PCM-Signai.e (Ip, Is) ist, die dem zumindest einen PCM/PWM-Umsetzer (2, 3, 20, 30) eingegeben werden,
der zumindest eine PCM/PWM-Umset.zer (2, 3, 20, 30) ein Doppelrampentyp ist,
der Aufwärts/Abwärtszähler, der von dem Taktsignal (E) gespeist ist und vom Aufwärts/Abwärtstyp ist, als Eingabe ein Rampeninversionssignal (D) hat und als Ausgabe ein digitales Vergleichssignal (Z) erzeugt bestehend aus der Anzahl von Bits (P, S) der digitalen PCM-Signale (Ip, Is), die dem zumindest einen PCM/PWM-Umsetzer (2, 3, 20, 30) eingegeben werden, in der Form einer Aufeinanderfolge von Aufwärts- und Abwärtsrampen bei einer halben Frequenz (Fin*k/2) verglichen mit der Frequenz der digitalen PCM-Signale (Ip, Is), die dem zumindest einen PCM/PWM-Umsetzer (2, 3, 20, 30) eingegeben werden, und
dadurch gekennzeichnet, dass
zwei identische Leistungsverstärkungsendstufen (101, 102) vorgesehen sind, die im Gegentakt arbeiten und bei denen das Invertieren des Signals, das dem invertierenden Eingang (-) der zwei Endstufen (101, 102) zugeführt wird, geschieht durch Verdoppeln des Paars von PCM/PWM-Doppelrampenumsetzern (2, 3) und Invertieren des Rampeninversionssignals (D) des Paars von PCM/PWM-Umsetzern (2, 3) und Speisen sowohl des Paars von PCM/PWM-Umsetzern (2, 3) als auch ihrer Duplikate (20, 30) mit denselben digitalen PCM-Signalen (Ip, Is) des ersten Busses und des zweiten Busses.

13. Verstärker nach Anspruch 12, **dadurch gekennzeichnet, dass** er enthält:

ein Mittel zum Invertieren des PWM-Signals (Os, Osn), das am Ausgang der PCM/PWM-Umsetzer (3, 30) des Paars (2, 3) und seines Duplikats (20,30), die mit den digitalen PCM-Signalen (Is) gespeist werden, die die niedrigerwertigen Bits (LSB) enthalten,
ein Mittel zum Dämpfen (200) der invertierten PWM-Signale und
ein Mittel zum Addieren jedes der PWM-Signale, die invertiert und gedämpft wurden, an dem invertierenden Knoten (-), an dem die PWM-Signale, die von zu dem anderen aus dem Paar (2, 3) von Umsetzern und seinem Duplikat (20, 30) gehörenden PCM/PWM-Umsetzern (2, 20) erzeugt werden, addiert werden.

14. Verstärker nach Anspruch 1, **dadurch gekennzeichnet, dass** der Oszillator (7) enthält
Inverter, von denen jeder aus einem Paar von MOS-Transistoren (M1, M2, M3, M4, M5, M6) gebildet ist und die in Serie in einer Schleife geschaltet sind, so dass der Eingang des ersten Inverters mit dem Ausgang des letzten Inverters verbunden ist,
Kapazitäten (C1, C2, C3) in der gleichen Anzahl wie die Inverter, wobei bei jedem ein Anschluss mit einem jeweiligen Eingang jedes Inverters verbunden ist und der andere Anschluss mit Masse verbunden ist, und
einen MOS-Transistor (Mr), der als Eingabe die Rücksetzpulse (IR) hat und dessen Ausgang mit dem Eingang des ersten Inverters verbunden ist"

Revendications

1. Amplificateur de puissance MID comprenant au moins un convertisseur MIC/MID (2, 3, 20, 30) qui est alimenté par des signaux d'entrée numériques MIC (Ip, Is) et produit des signaux de sortie numériques MID (Op, Os, Opn, Ops), et au moins un étage final (10, 101, 102) d'amplification de puissance des signaux numériques MID (Op, Os, Opn, Ops) en sortie dudit au moins un convertisseur MIC/MID (2, 3, 20, 30), ledit au moins un convertisseur MIC/MID (2, 3, 20, 30) comprenant un compteur progressif ou un compteur réversible alimenté avec au moins un signal d'horloge (E) produit par un dispositif de générateur d'horloge (5) et comprenant un comparateur numérique (8) approprié pour comparer lesdits signaux d'entrée numériques MIC (Ip, Is) dudit au moins un convertisseur MIC/MID (2, 3, 20, 30) avec un signal de comparaison numérique (B, Z) produit par ledit compteur progressif ou ledit compteur réversible et produisant en sortie lesdits signaux numériques MID (Op, Os, Opn, Ops),
caractérisé en ce que
ledit dispositif de générateur d'horloge (5) comprend un dispositif de générateur d'impulsions (6) et un oscillateur (7), ledit dispositif de générateur d'impulsions (6) recevant un signal à une fréquence (Fin*k) égale à la fréquence desdits signaux d'entrée numériques MIC (Ip, Is) dudit au moins un convertisseur MIC/MID (2, 3, 20, 30) et produisant des impulsions de réinitialisation de sortie (IR), lesdites impulsions de réinitialisation (IR) étant envoyés à l'entrée dudit oscillateur (7) produisant comme sortie ledit au moins un signal d'horloge (E).

2. Amplificateur selon la revendication 1,
caractérisé en ce qu'il comprend un bloc de suréchantillonnage et de mise en forme du bruit (1) recevant des premiers signaux d'entrée numériques MIC (In) organisés en mots avec un nombre donné de bits (M) et à une fréquence donnée (Fin) et produisant comme sortie des deuxièmes signaux numériques MIC (Ip, Is) organisés en mots composés d'un nombre de bits (N) inférieur audit nombre donné

de bits (M) et à une fréquence multiple (Fin*k) par rapport à ladite fréquence donnée (Fin) des premiers signaux d'entrée numériques MIC (In), lesdits deuxièmes signaux numériques MIC (Ip, Is) étant les signaux numériques MIC en entrée sur ledit au moins un convertisseur MIC/MID (2, 3, 20, 30).

3. Amplificateur selon la revendication 2, **caractérisé en ce qu'**il comprend un premier bus approprié pour transmettre des premières données numériques MIC (Ip) contenant un premier nombre (P) de bits de poids fort (MSB) desdits deuxièmes signaux numériques MIC (Ip, Is) et un deuxième bus approprié pour transmettre des deuxièmes données numériques MIC (Is) contenant un deuxième nombre (S) de bits de poids faible (LSB) desdits deuxièmes signaux numériques MIC (Ip, Is), et **caractérisé en ce qu'**il prévoit des premier (2, 20) et deuxième (3, 30) convertisseurs MIC/MID alimentés respectivement par lesdites premières (Ip) et deuxièmes (Is) données numériques MIC et produisant en sortie respectivement des premier (Op, Opn) et deuxième (Os, Osn) signaux MID.

4. Amplificateur selon la revendication 3, **caractérisé en ce que** ledit deuxième signal MID (Os, Osn) est préalablement atténué par un rapport équivalent à la puissance en base deux du deuxième nombre (S) de bits de poids faible (LSB) transmis par ledit deuxième bus à l'entrée dudit deuxième convertisseur MIC/MID (3, 30) et est additionné audit premier signal MID (Op, Opn) au niveau d'un noeud d'inversion (-) dudit au moins un étage final d'amplification de puissance (10, 101, 102) de l'amplificateur.

5. Amplificateur selon la revendication 1, **caractérisé en ce que** ledit au moins un générateur d'horloge (5) produit un signal d'horloge (E) dont la fréquence (Fclock) est égale au produit de la fréquence (Fin*k) des bits des signaux numériques MIC (Ip, Is) comme entrée sur ledit au moins convertisseur MIC/MID (2, 3, 20, 30) par la fréquence de base deux du nombre de bits (P, S) desdits signaux numériques MIC (Ip, Is) entrés sur au moins un convertisseur MIC/MID (2, 3, 20, 30), ledit compteur progressif ou ledit compteur réversible alimenté par ledit au moins un signal d'horloge (E) générant un signal de sortie de comparaison numérique (B, Z) composé dudit nombre de bits (P, S) sous la forme d'au moins une rampe de valeurs numériques à une fréquence identique ou à une demi-fréquence comparée à ladite fréquence (Fin*k) de bits des signaux numériques MIC (Ip, Is) en entrée sur le au moins un convertisseur MIC/MID (2, 3, 20, 30).

6. Amplificateur selon la revendication 5, **caractérisé en ce que** ledit signal de comparaison numérique (B) dudit au moins un convertisseur MIC/MID (2, 3, 20, 30) est sous la forme d'une succession de rampes montantes de valeurs numériques à une fréquence identique à ladite fréquence (Fin*k) de bits des signaux numériques MIC (Ip, Is) entrés sur au moins un convertisseur MIC/MID (2, 3, 20, 30).

7. Amplificateur selon la revendication 5, **caractérisé en ce que** ledit au moins un convertisseur MIC/MID (2, 3, 20, 30) est du type double rampe, ledit compteur réversible étant du type compteur/décompteur, ayant comme entrée un signal dInversion de rampe (D) et générant comme sortie un signal de comparaison numérique (Z) composé par le nombre de bits (P, S) desdits signaux numériques MIC (Ip, Is) entrés sur au moins un convertisseur MIC/MID (2, 3, 20, 30) sous la forme d'une succession de rampes montantes et descendantes à une demi-fréquence (Fin*k/2) comparée à la fréquence des signaux numériques MIC (Ip, Is) entrés sur ledit au moins un convertisseur MIC/MID (2, 3, 20, 30).

8. Amplificateur selon la revendication 1 ou 4, **caractérisé en ce qu'**il prévoit un seul étage final d'amplification de puissance (10).

9. Amplificateur selon la revendication 1 ou 4, **caractérisé en ce qu'**il prévoit deux étages finaux d'amplification de puissance identiques (102, 102) fonctionnant en phase contraire et où l'inversion du signal envoyé vers l'entrée d'inversion desdits deux étages finaux est effectuée en inversant le signal numérique MID (Op, Os) sorti dudit au moins un convertisseur MIC/MID (2, 3).

10. Amplificateur selon la revendication 1 ou 4, **caractérisé en ce qu'**il prévoit deux étages finaux d'amplification de puissance identiques (101, 102) fonctionnant en phase contraire et où l'inversion du signal envoyé vers l'entrée d'inversion (-) desdits deux étages finaux (101, 102) est effectuée en dupliquant ledit au moins un convertisseur MIC/MID (2, 3) et en inversant les signaux numériques MIC (Ip, Is) entrés sur lesdits au moins deux convertisseurs MIC/MID (2, 3).

11. Amplificateur selon les revendications 1 et 4, **caractérisé en ce que** ledit au moins un générateur d'horloge (5) produit un signal d'horloge (E) dont la fréquence (Fclock) est égale au produit de la fréquence (Fin*k) des bits des signaux numériques MIC (Ip, Is) entrés sur ledit au moins un convertisseur MIC/MID (2, 3, 20, 30) par la puissance de base deux du nombre de bits (P, S) desdits signaux numériques MIC (Ip, Is) entrés sur au moins un convertisseur MIC/MID (2, 3, 20, 30), ledit au moins un convertisseur MIC/MID (2, 3, 20, 30) est du type double ram-

pe, ledit compteur réversible étant alimenté par ledit signal d'horloge (E) et étant du type compteur/décompteur, ayant comme entrée un signal de d'inversion de rampe (D) et générant comme sortie un signal de comparaison numérique (Z) composé du nombre de bits (P, S) desdits signaux numériques MIC (Ip, Is) entrés sur au moins un convertisseur MIC/MID (2, 3, 20, 30) sous la forme d'une succession de rampes montantes et descendantes à une demi-fréquence (Fin*k/2) comparée à la fréquence des signaux numériques MIC (Ip, Is) entrés sur ledit au moins un convertisseur MIC/MID (2, 3, 20, 30), et **caractérisé en ce qu'**il prévoit deux étages finaux d'amplification de puissance identiques (101, 102) fonctionnant en phase contraire et où l'inversion du signal envoyé vers l'entrée dInversion (-) desdits deux étages finaux (101, 102) est effectuée en dupliquant ledit au moins un convertisseur à double rampe MIC/MID (2, 3) et en inversant le signal d'inversion de rampe (D) dudit au moins un convertisseur MIC/MID (2, 3) et en alimentant ledit au moins un convertisseur MIC/MID (2, 3) et son double (20, 30) avec les mêmes signaux numériques d'entrée MIC (Ip, Is).

12. Amplificateur selon la revendication 4, **caractérisé en ce que** ledit au moins un générateur d'horloge (5) produit un signal d'horloge (E) dont la fréquence (Fclock) est égale au produit de la fréquence (Fin*k) des bits des signaux numériques MIC (Ip, Is) en entrée sur ledit au moins un convertisseur MIC/MID (2, 3, 20, 30) par la puissance de base deux du nombre de bits (P, S) desdits signaux numériques MIC (Ip, Is) entrés sur au moins un convertisseur MIC/MID (2, 3, 20, 30), ledit au moins un convertisseur MIC/MID (2, 3, 20, 30) étant du type double rampe, ledit compteur réversible étant alimenté par ledit signal d'horloge (E) et étant du type compteur/décompteur, ayant comme entrée un signal d'inversion de rampe (D) et générant en sortie un signal de comparaison numérique (Z) composé du nombre de bits (P, S) desdits signaux numériques MIC (Ip, Is) entrés sur au moins un convertisseur MIC/MID (2, 3, 20, 30) sous la forme d'une succession de rampes montantes et descendantes à une demi-fréquence (Fin*k/2) comparée à la fréquence des signaux numériques MIC (Ip, Is) entrés sur ledit au moins un convertisseur MIC/MID (2, 3, 20, 30), et **caractérisé en ce qu'**il prévoit deux étages finaux d'amplification de puissance identiques (101, 102) fonctionnant en phase contraire et où l'inversion du signal envoyé vers l'entrée d'inversion (-) desdits deux étages finaux (101, 102) est effectuée en dupliquant ledit couple de convertisseurs à double rampe MIC/MID (2, 3) et en inversant le signal d'inversion de rampe (D) dudit couple de convertisseurs MIC/MID (2, 3) et en alimentant ledit couple de convertisseurs MIC/MID (2, 3) et son double (20, 30) avec les mêmes signaux numériques MIC (Ip, Is) dudit premier bus et dudit deuxième bus.

13. Amplificateur selon la revendication 12, **caractérisé en ce qu'**il comprend un moyen pour inverser les signaux MID (Os, Osn) produits à la sortie des convertisseurs MIC/MID (3, 30) dudit couple (2, 3) et de son double (20, 30) qui sont alimentés avec lesdits signaux numériques MIC (Is) contenant les bits de poids faible (LSB), un moyen pour atténuer (200) les signaux MID inversés et un moyen pour additionner chacun desdits signaux MID inversés et atténués sur le noeud d'inversion (-) sur lequel les signaux MID produits par les convertisseurs MIC/MID (2, 20) appartenant à l'autre couple entre ledit couple (2, 3) de convertisseurs et son double (20, 30) sont additionnés.

14. Amplificateur selon la revendication 1, **caractérisé en ce que** ledit oscillateur (7) comprend des inverseurs, chacun formé par un couple de transistors MOS (M1, M2 ; M3, M4 ; M5, M6) et placé en série et dans une boucle de sorte que l'entrée du premier desdits inverseurs soit reliée à la sortie du dernier desdits inverseurs, des capacités (C1, C2, C3) dans un nombre égal à celui des inverseurs et chacune ayant une borne reliée à une entrée respective de chaque inverseur et l'autre borne mise à la terre, un transistor MOS (Mr) ayant comme entrée lesdites impulsions de réinitialisation (IR) et la sortie reliée à l'entrée dudit premier inverseur.

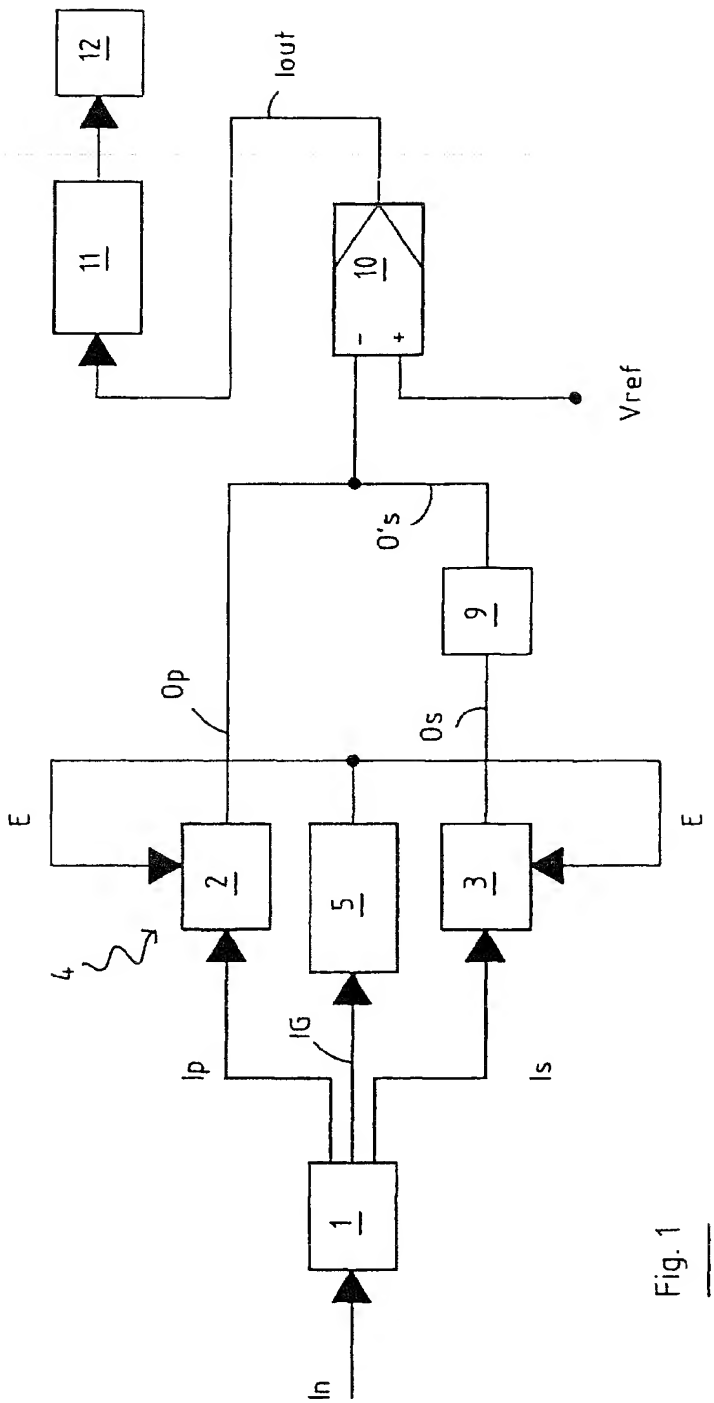

Fig. 1

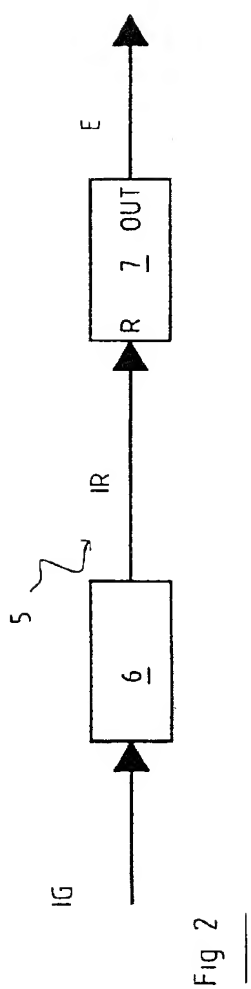

Fig 2

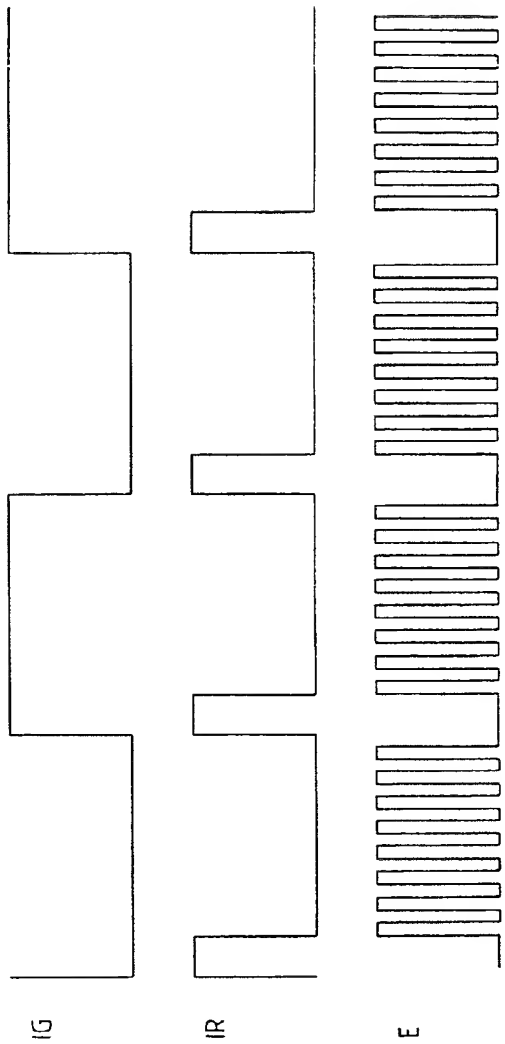

Fig. 3

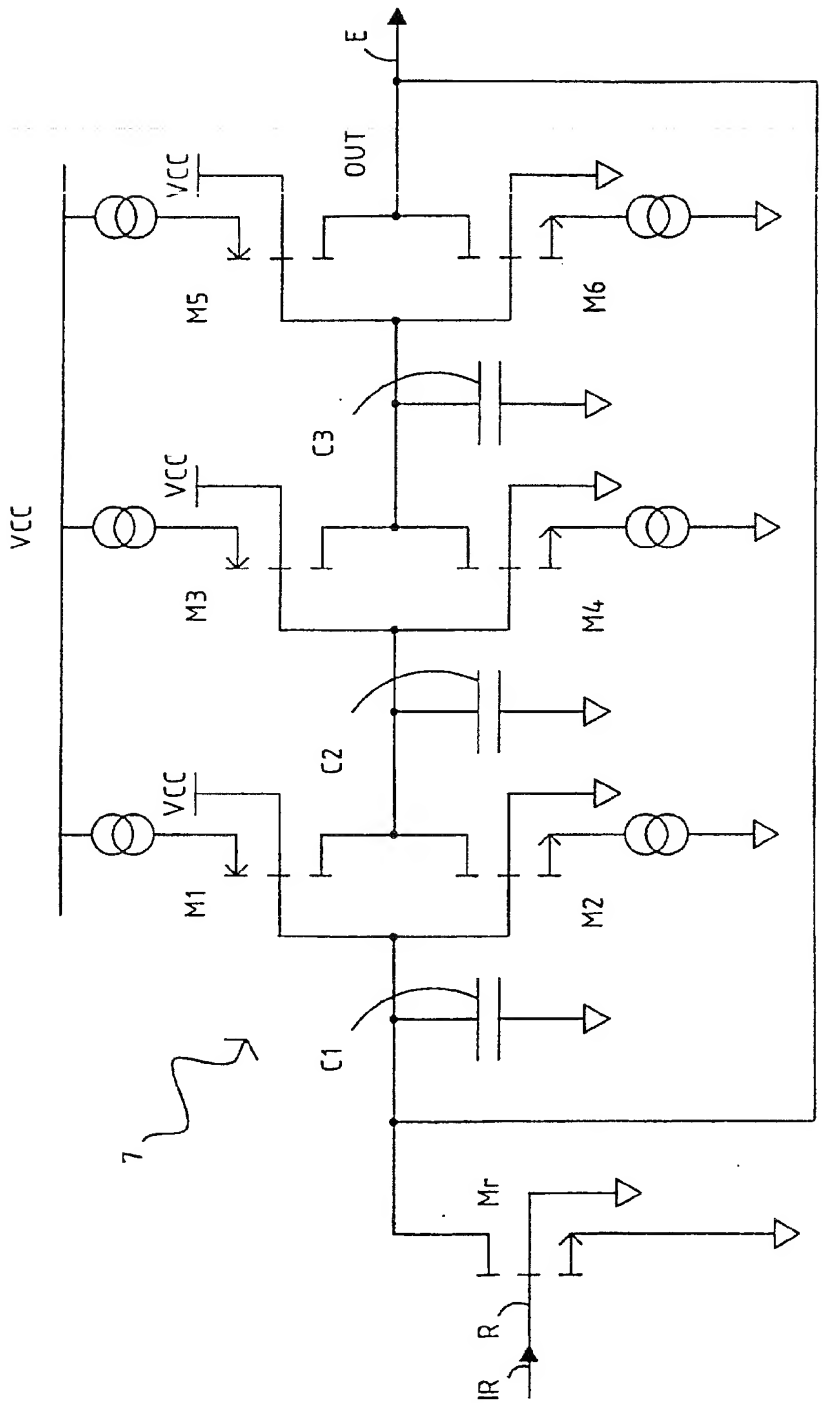

Fig. 4

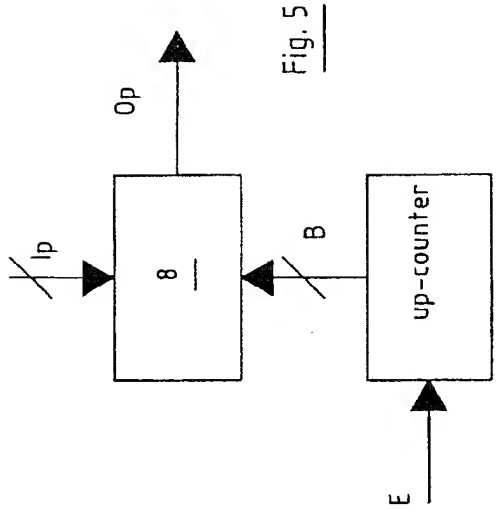

Fig. 5

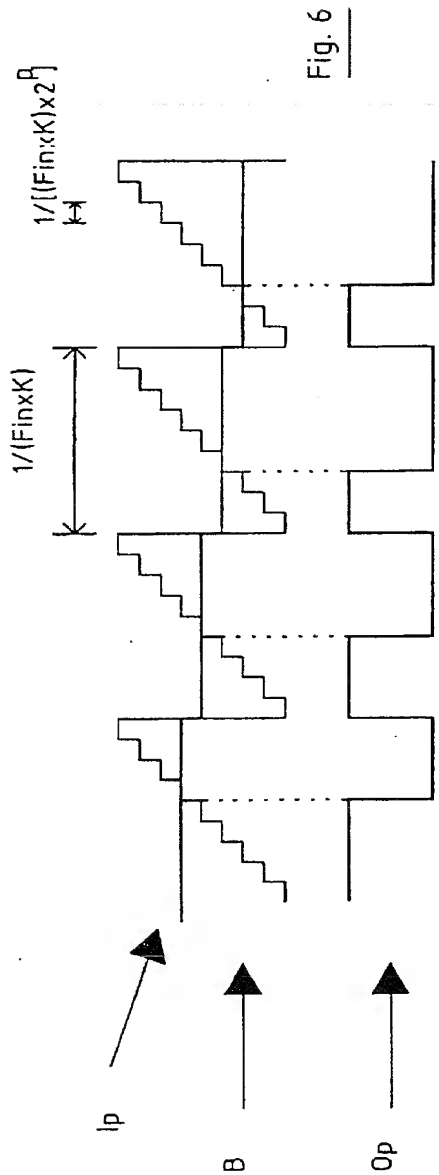

Fig. 6

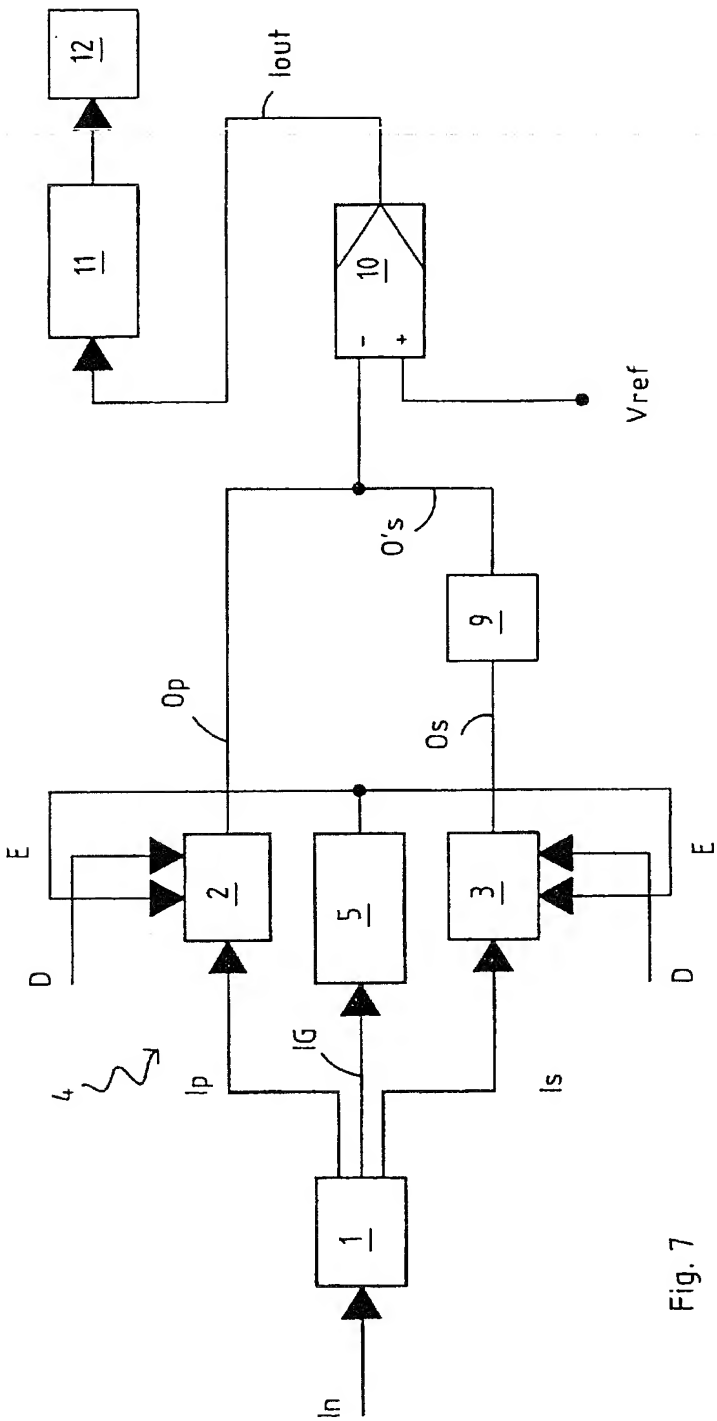

Fig. 7

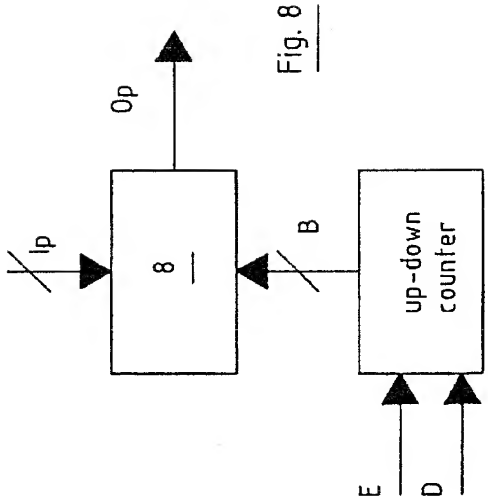

Fig. 8

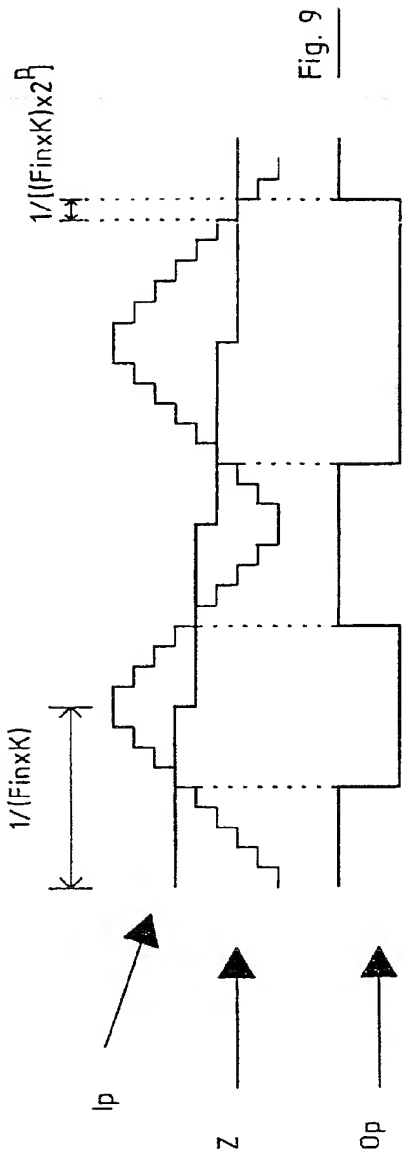

Fig. 9

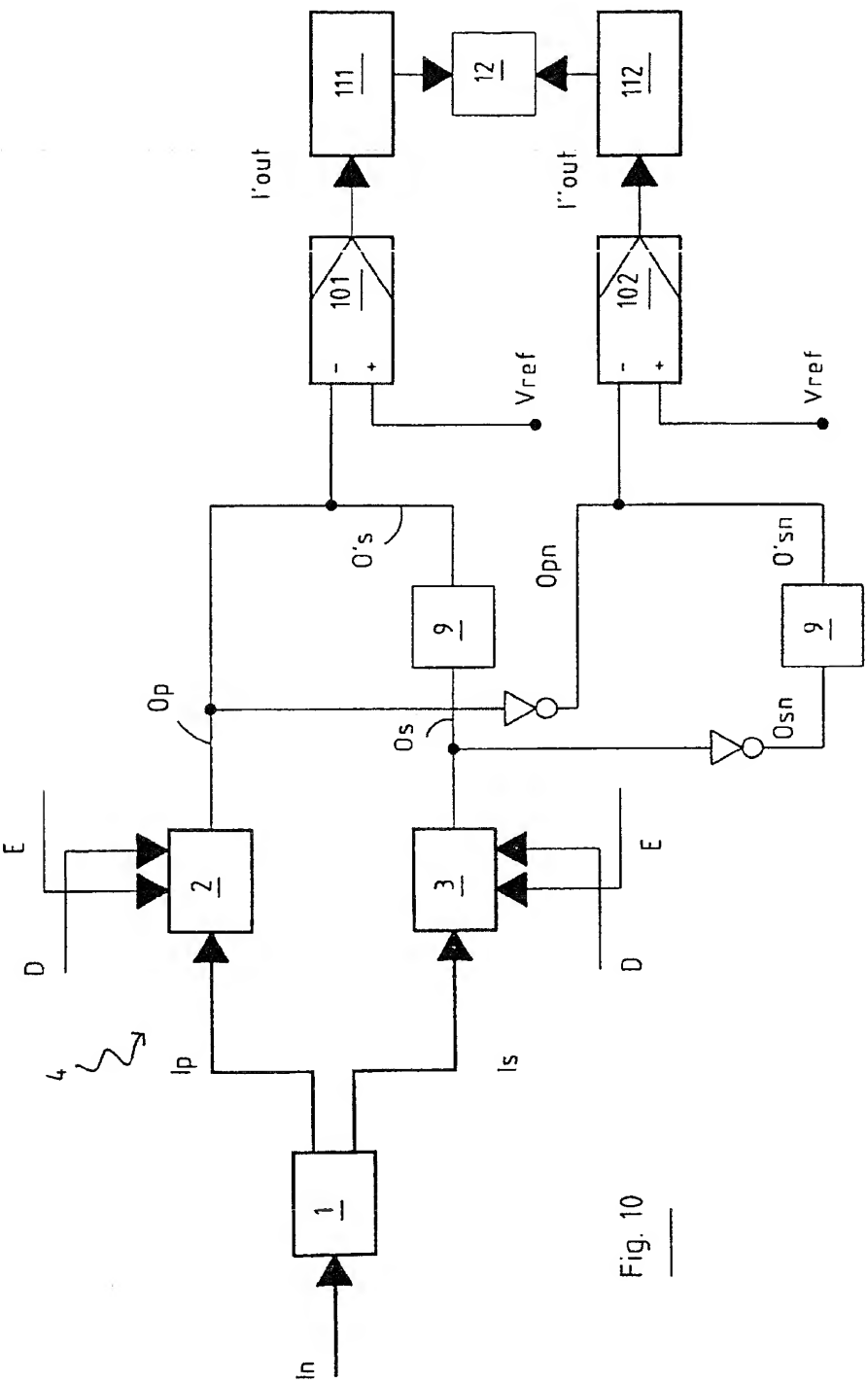
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Fig. 10

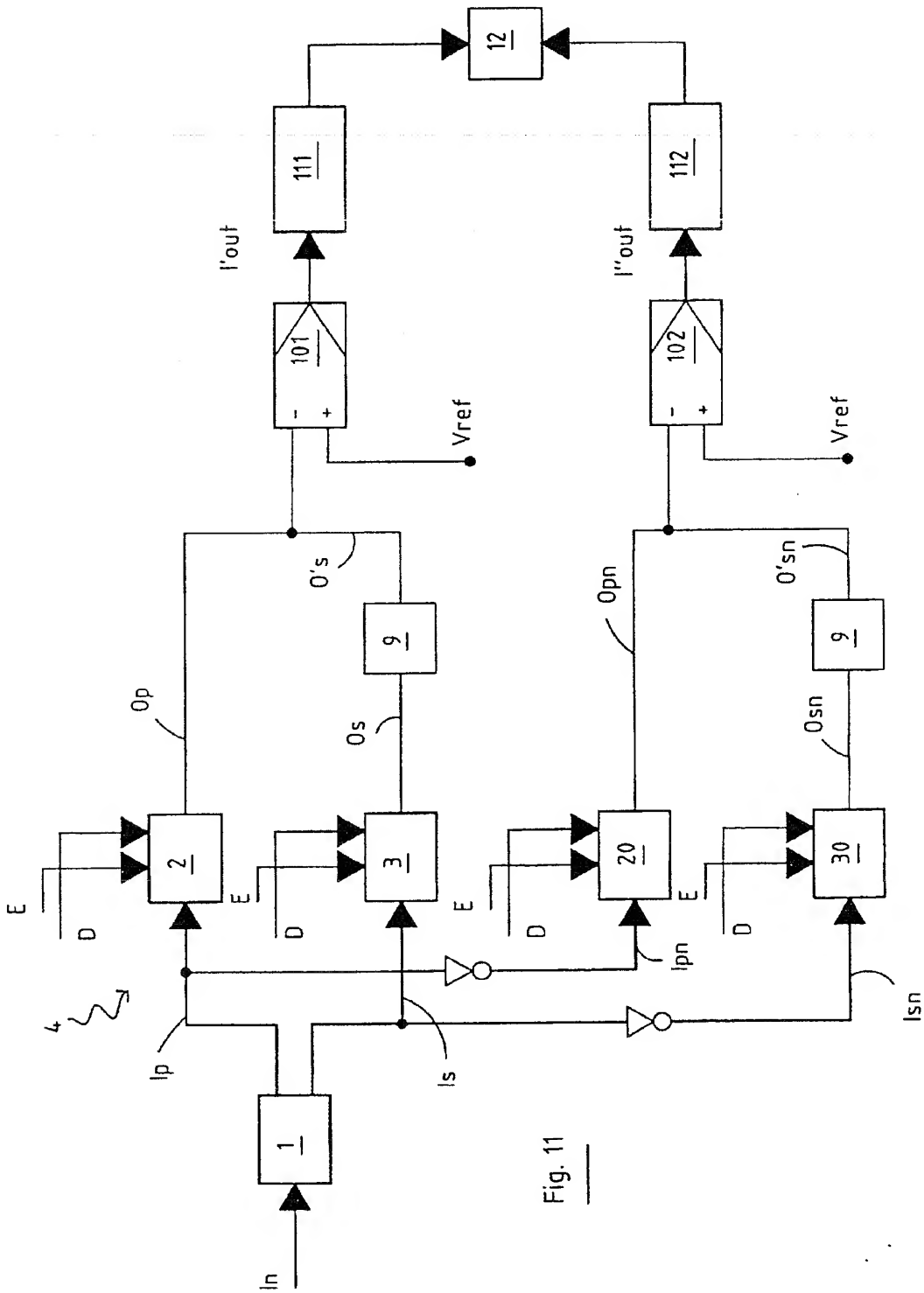
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Fig. 11

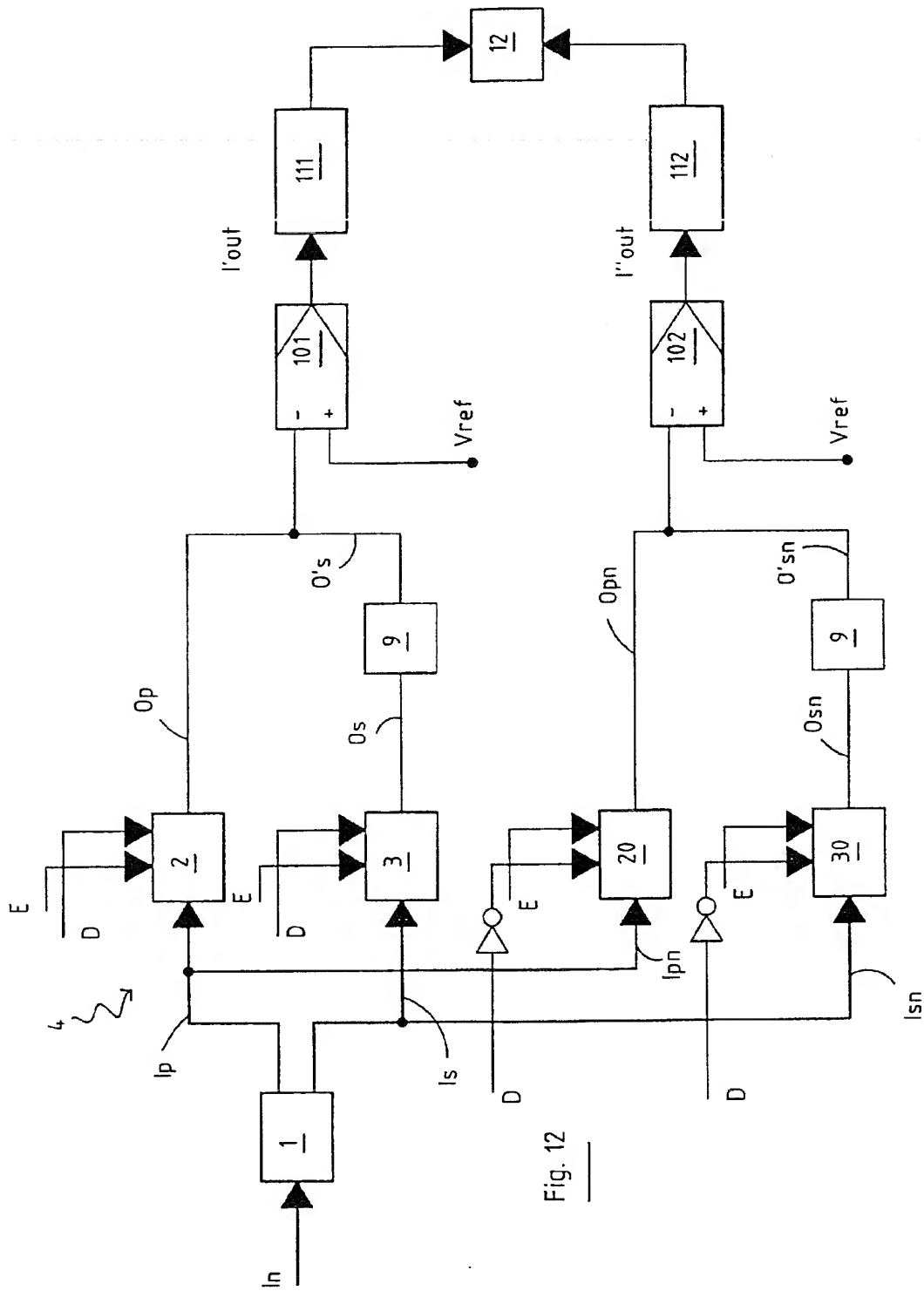
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Fig. 12

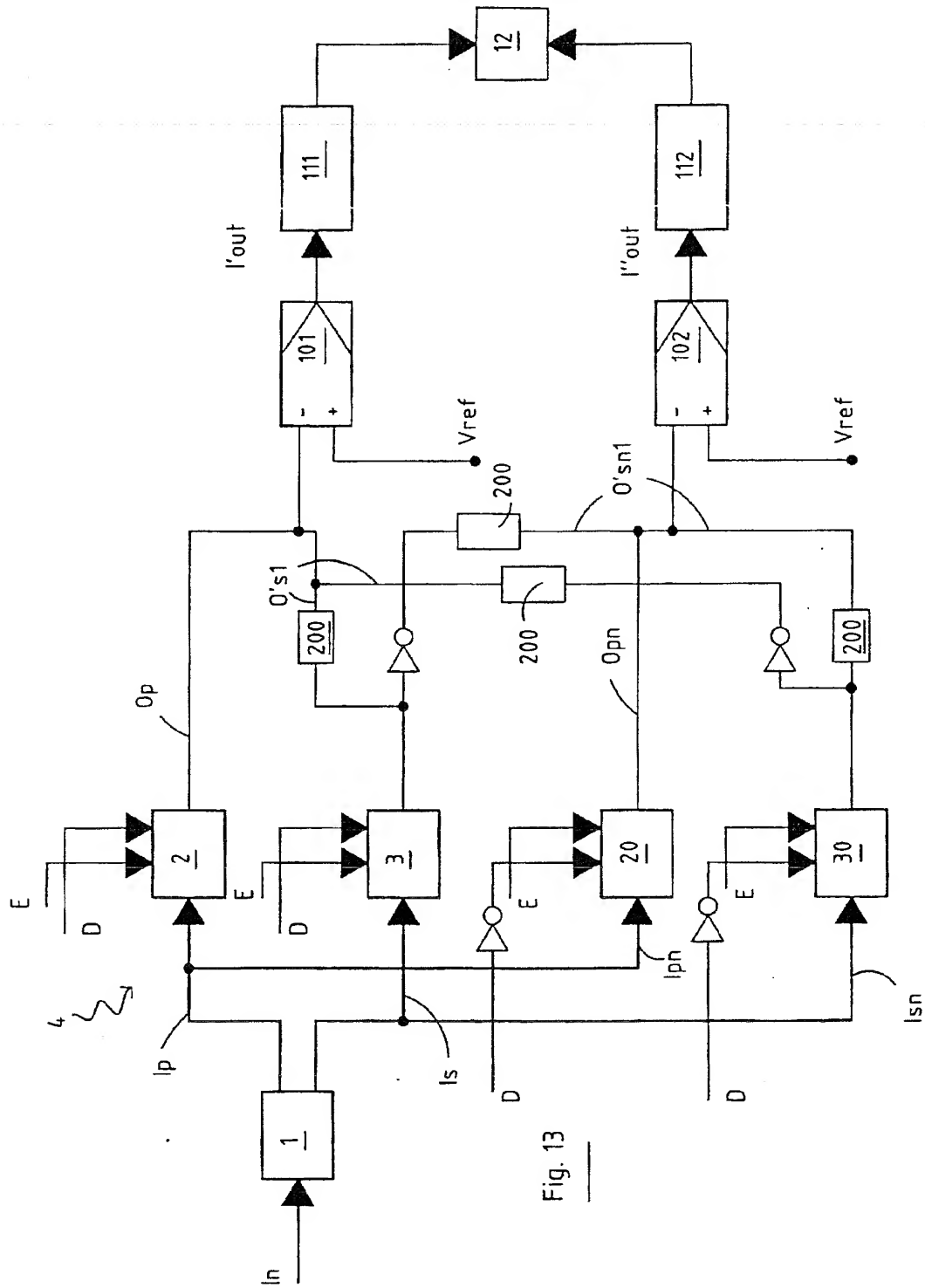
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Fig. 13